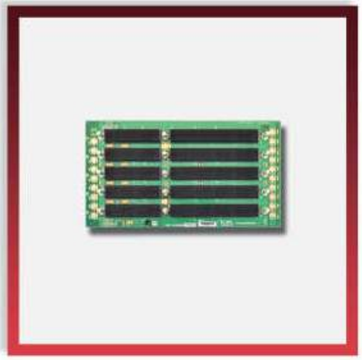
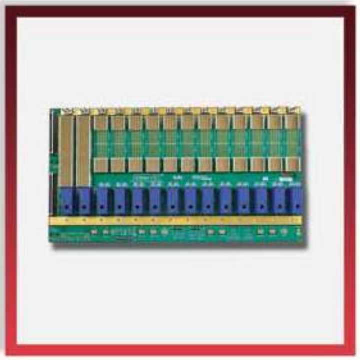
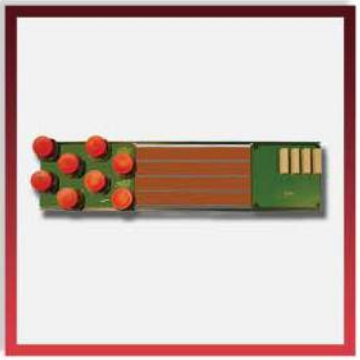
ELMA BUSTRONIC

Elma Bustronic


OpenVPX

VME, VME64x,
VXS


AdvancedTCA,
MicroTCA



CompactPCI, 2.16

Custom Designs

High Performance Backplanes and System Accessories

System Accessories

ELMA
Your Solution Partner

COMPANY PROFILE

ABOUT ELMA BUSTRONIC

Elma Bustronic is the industry expert in high-performance backplanes and related system accessories. Focused on backplanes, Elma Bustronic offers customers a unique level of design and manufacturing expertise, industry knowledge, and clarity of purpose not found elsewhere in the marketplace. The company is therefore on the leading edge of design innovations and new standardized backplane architecture development while forging key partnerships with other industry leaders.

Our standard product portfolio includes AdvancedTCA, CompactPCI/2.16, MicroTCA, OpenVPX, VME/64x, VXS, and more. Elma Bustronic also offers SFF (Small Form Factor), rigid-flex, and RTM designs, as well as various test/development accessories. Services offered by the company include contract assembly/build-to-print, simulation, testing, and custom design.

Elma Bustronic's design engineers are experts at developing custom backplanes to meet your specifications, from initial concept to volume production. These designs serve a wide array of industries, including aerospace, military, industrial automation, telecommunications, medical, and high-performance computers.

Since 2000, Elma Bustronic and European sister-company Elma TreNew have been leveraging each other's expertise and when appropriate, sharing resources. This combination offers one of the best teams in high-speed and high-complexity backplanes in the world. Elma Bustronic and Elma Electronic Inc. have their USA design and production headquarters conveniently side-by-side in Fremont CA. Elma offers system solutions from chassis platforms to fully integrated systems. Whether you prefer only a backplane or a turnkey chassis platform or an integrated system, we'll provide the level of service that suits your requirements.

ELMA OFFERS

Elma Electronic offers also an extensive line of fully tested System Platforms (combining standard and/or custom mechanics, backplanes, power supplies and cooling), enclosures and chassis for 19" rack mount, cabinet enclosures/consoles and front panels, handles, switches, LEDs and knobs. Visit www.elma.com to get an overview of all of Elma's products.

ELMA PRODUCT DIVISIONS

System Solutions

Backplanes

Chassis Platforms, Embedded Products & Integrated Systems

Cabinets

Enclosures and Components

Enclosure Kits & Cases, Front Panels & Ejector Handles

Rotary Switches

Switches/Encoders, Knobs and LEDs

INDUSTRIES

Communications
Military and Aerospace
Medical
Transportation
Scientific and Research
Security
Test and Measurement
Industrial

WHY CHOOSE ELMA BUSTRONIC

- Vast experience in various open and custom architectures
- Renowned quality and design expertise
- State of the art assembly and testing equipment
- Local service, global reach
- In-house design, production, & testing
- Flexibility - excellent service whether you buy one piece or one thousand

USA - Elma Bustronic Headquarters

USA - Elma Headquarters

USA - Lathrop

USA - Pennsylvania

Global Locations

Lawrenceville, GA USA - Optima EPS, An Elma Company
Wetzikon, Switzerland - Elma Electronic AG
Pforzheim, Germany - Elma Trenew Electronic GmbH
Villemoirieu, France - Elma Electronic France SA
Shanghai, China - Elma Electronic China
Sgula Petach Tikva, Israel - Elma Electronic Israel Ltd.
Bedford, UK - Elma Electronic UK Ltd.
Singapore, Asia Pacific - Elma Asia Pacific Pte. Ltd.

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ELMA BUSTRONIC COMPANY PROFILE

VITA BACKPLANES

PICMG BACKPLANES

OTHER BACKPLANES

ACCESSORIES

Elma Bustronic Company Profile

Focused on backplanes, Elma Bustronic Corporation delivers high-performance products that are unsurpassed in design and quality. From custom designs to standard configurations, we provide the best in backplane technology serving the communications, military/aerospace, computer, instrumentation, industrial automation, and medical industries. Our expertise includes architectures in OpenVPX, AdvancedTCA, CompactPCI/2.16, MicroTCA, VME/64x, VPX, VXS and more. We also have extensive experience with custom and high-speed buses and fabrics. With speeds hitting 40Gbps per channel, Elma Bustronic has continued to expand our expertise in simulation, characterization, and model extraction.

Design and Engineering

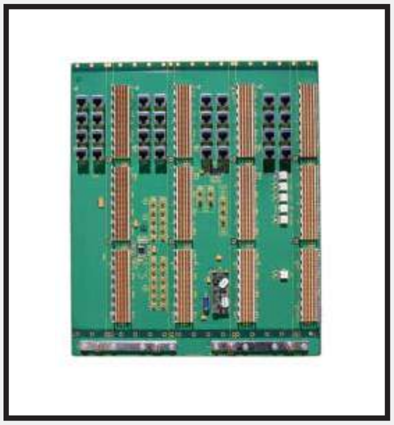
The Elma Bustronic design and engineering team is often regarded as the best in the business. The Elma Bustronic team has constantly delivered innovative and intelligent solutions. The company has been the recognized leader in Switched Fabric designs, having developed the first PICMG 2.16 (Compact Packet Switching), PICMG 2.17 (StarFabric), VXS, AdvancedTCA and VPX backplanes on the market. Our leadership and expertise in the VITA and PICMG committees keeps us on the cutting edge of technology. With over 300 custom designs under our belt, Elma Bustronic can find a solution to almost any requirement you may have.

Design Center in Europe

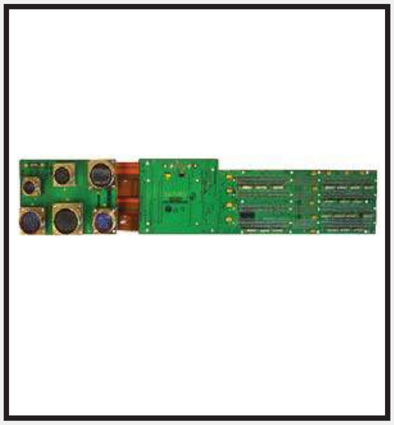
Elma Bustronic's sister company, Elma Trenew is located in Germany, with several designers and engineers specializing in backplanes. Our European design and engineering staff are renowned for their experience in complex telecom backplanes with high layer counts, rigid-flex-rigid backplanes, active cards and backplanes, high-speed differential signals, switched fabrics, and hot swap solutions.

Custom Backplane Examples

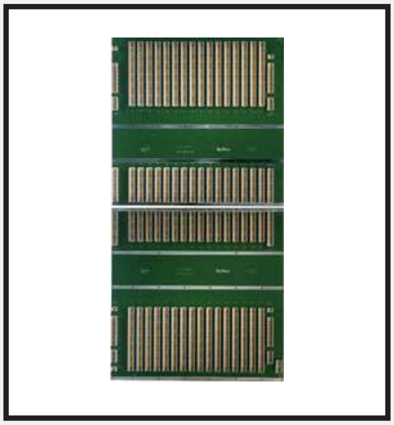
Elma Bustronic is a global leader in customized backplanes with over 3,000 unique designs to date. Below are a few brief examples.



"Scientific" Backplane for Columbia University's 1024 Node SuperComputer for DOE



Rigid Flex



Telecom II

Elma Bustronic Backplane Signal Integrity Initiative (SII)

With the advancement of newer multi-gigabit specifications (10GBASE-KR, 40GBASE-KR4, CEI-28G-VSR, etc), performing signal integrity analysis for backplane channels becomes not only recommendable, but mandatory. Pre-layout and post-layout simulations as well as actual lab measurements, followed by studies correlating the simulations with measurements should be in the toolkit of any designer working in the multi-gig channel realm. Backplanes present unique challenges with regard to embedding/de-embedding certain portions of a backplane channel and the accuracy in performing simulations and measurements to properly compare models to test results is crucial.

Elma Bustronic uses the following tools:

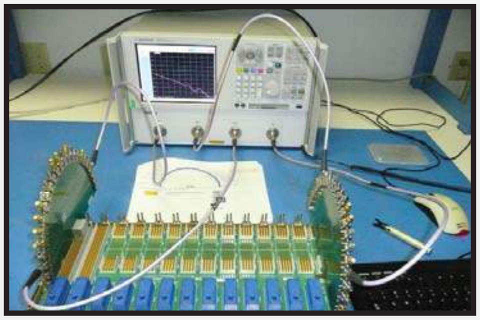
- Ansoft HFSS
- Ansoft DesignerSI
- HP 54750 TDR
- Specially designed probe cards
- Agilent N5230A 20 GHz VNA

Examples of possible measurement characteristics:

- Impedance for single ended and differential lines
- Cross-Talk
- Propagation Delay
- S-parameters
- Eye Diagram

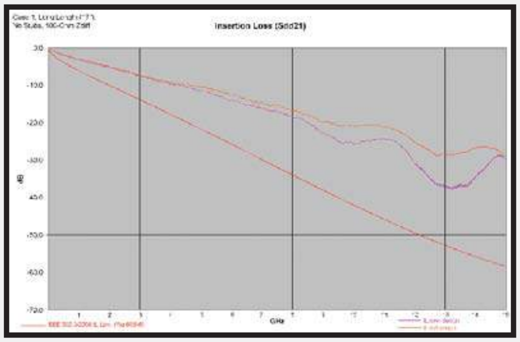
Examples of possible simulation characteristics:

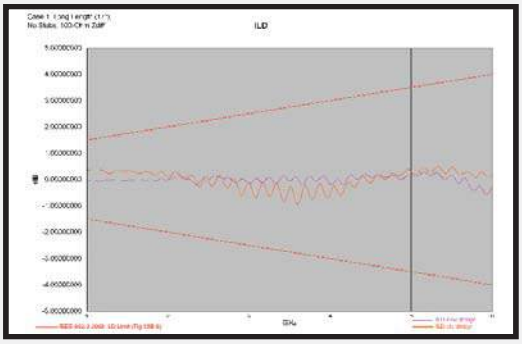
- Impedance
- Cross-Talk
- Propagation Delay
- Attenuation
- Insertion & Return Loss
- Eye Diagram



Above: Characterization of 14-slot ATCA backplane using Elma Bustronic's unique probe card.

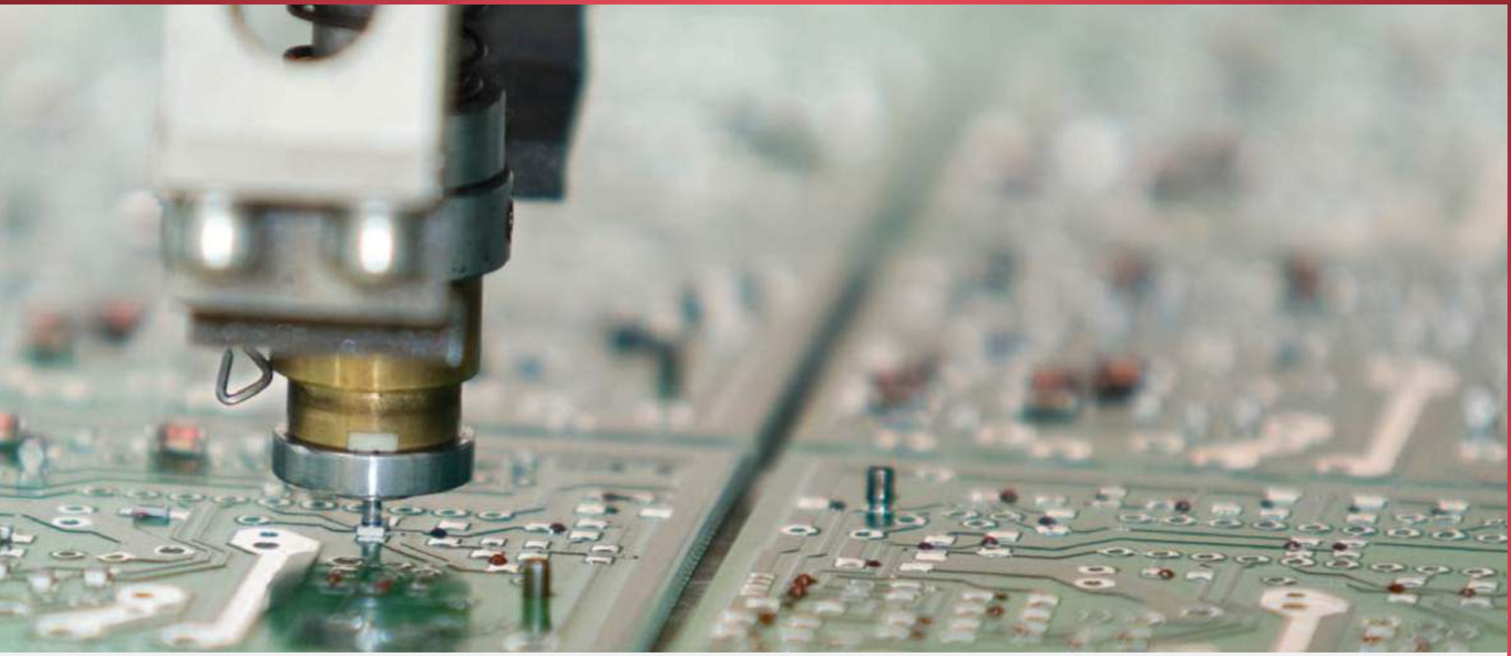
Top Left: Insertion loss measurement
Bottom Left: ILD measurement





The S-parameter models come from extracted empirical models captured by VNA and software driven TDT measurement techniques as well as the synthesized output of specialized 3D field solvers. The result is more accurately characterized via structures, accurate channel models and a more precise representation of layout transition features and unavoidable stubs.

Measurement, model extraction, and simulation services Elma Bustronic offers services to characterize the interconnect path and provide models of representative circuit paths. These models can be used to generate reports that confirm the performance of these backplanes and also allow full system simulations to be performed that will help in the design process. Elma Bustronic can also provide the integration of measurement-derived models into the application engineering process. This includes the ability to easily generate eye-patterns based on the customer's specific requirements including such questions as signal degradation through backplane IO connectors and specific lengths of I/O cabling.



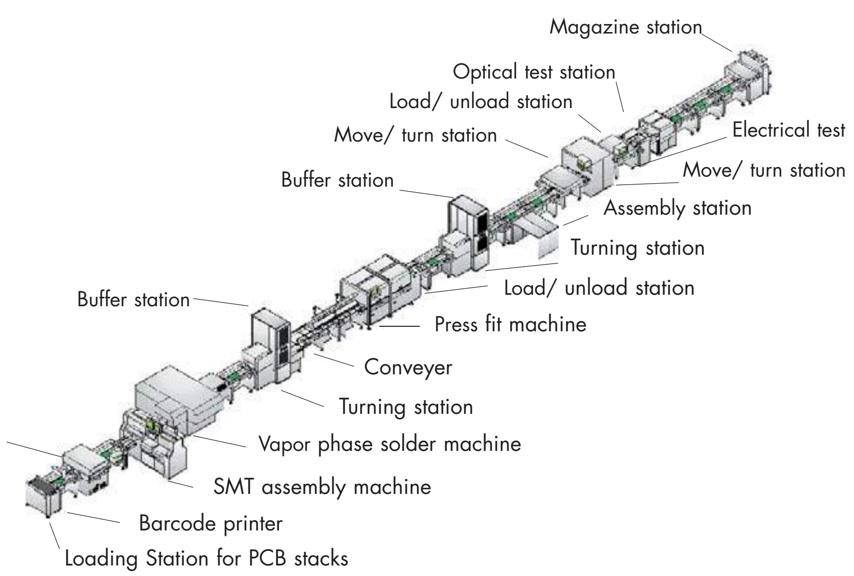
The following equipment will be part of Elma Bustronic's assembly line in early 2012:

Automated Optical Inspection
Optical inspection equipment for co-planarity testing of BGA and CSP devices and enhanced solder paste measurement capability. Has five camera desktop AOI system, 9.8 micron pixel resolution, marking system, and barcode reader.

Selective Soldering
Precision solder for small boards and components. Programmable to set all process parameters, including immersion depths, pre-heat dwells, travel distances and speeds, solder temperature and wave height.

Laser Marking System
The laser marking system is fully programmable with servo controlled motion axis.

The Automated Assembly Line in Germany
For special projects, we are able to use our automated assembly line in Germany. Over 40 meters long, the line includes SMT assembly, vapor phase soldering, press fit capability, electrical, and optical testing. The facility is located in Pforzheim, Germany.



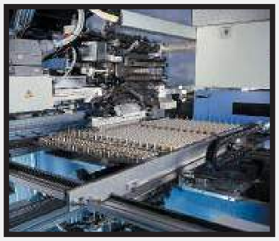
PRODUCTION CAPABILITIES

The Automated Assembly Line can support PCB sizes of up to 31.50" x 23.62" and thickness of up to 0.315". The SMT machines can assemble up to 10,000 components/hr with .03 mm precision. The Pressfit Assembly portion of the line has a cycle time of 3-5 seconds with 0.2 mm precision. Electrical and Optical testing can be performed including up to 21,620 electrical test points and a speed of 1000 measurements per second.

Automatic Assembly Line

SMT Assembly

Pressfit Assembly

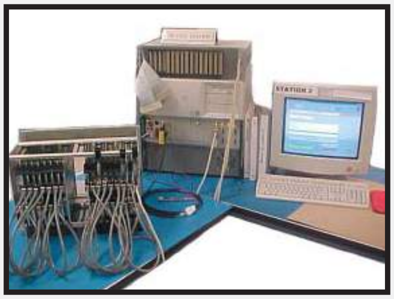


Electrical Test

Optical Test

Vapor Phase Soldering

QUALITY & TESTING



Quality is a top priority at Elma Bustronic and we have been an ISO 9001 certified company since 1997, and are currently certified to the more stringent ISO9001-2008 standards. We are always searching for new ways to improve our already outstanding product quality.

Investing substantially in state-of-the-art testing technology allows Elma Bustronic to deliver the quality our customers have come to expect. Testing systems include driver hardware and test-point electronics in extremely high-density packaging, which enable full, simultaneous testing of dense, high pin-count connectors on backplane slots. The network connection allows engineers to download and upload test programs without disrupting backplane testing, making the process virtually seamless.

Sharing resources with our Elma team in Europe gives Elma Bustronic one of the most impressive combined measurement and testing capabilities you can find. Elma Bustronic and Elma TreNew have integrated our engineering resources, including use of modeling systems, testing equipment, mechanical drawing software, measurement devices, and more.

X-ray Inspection Machine (Scienscope)

The x-ray inspection system provides a way to ensure proper and consistent soldering. With the ability to see under the surface of the BGA or other soldered component, the unit ensures that we don't have any opens or shorts, have proper solder filling, etc. The X-scope features a wide inspection area with tilting x-ray tube and detector capability. It also has computer controlled kV and mA settings and variable speed X-Y stage. The benefit is high spatial contrast, maximum magnification at even extreme angles, higher inspection speed, and ability to detect subtle density/grayscale differences.

SMT Line

The Elma Bustronic SMT line is over 80' long and includes an in-line printer, a pick-and-place SMT assembly machine, re-flow soldering system, and a multi-solvent backplane cleaning machine. Our customers benefit with faster turnaround times, increased volume and board complexity capabilities, and higher precision quality.

SMT2220 In-Line Printer

The production line utilizes a SMT2220 In-Line printer for pick-and-place SMT assembly.

Samsung Advanced Component Placer

The Samsung Advanced Component Placer can place 21,000 Components Per Hour (CPH) utilizing the Dual Servo-Flying Vision System with Sliding Type Feeders. This machine can handle small components and BGAs and boards up to 20" x 24".

Thermal Processing Oven (Blue M)

The oven is used for pre-baking, drying, and curing. We pre-bake the backplanes and boards to get rid of moisture inside the PCB. This helps provide more reliable soldering and functionality. After washing the unit, boards can also be dried or cured in the processing oven. The Blue M oven features superior heat ramp up and recovery, thick insulation for uniformity, and consistent/efficient heating.

Vitronics Soltec Thermal Processing System

The Vitronics Soltec XPM thermal processing system produces outstanding levels of uniformity and repeatability in solder re-flow.

The Nu/Clean 318 Aqueous Cleaner

This Nu/Clean 318 Cleaner is a high-pressure DI-Water base cleaner. It has a pre-wash chamber with 32 high-pressure spray nozzles, the wash chamber has 64 high-pressure spray nozzles, the rinse chamber has 80 high-pressure spray nozzles and the final rinse chamber has 12 high-pressure spray nozzles.

Rework Station (VJ Electronix)

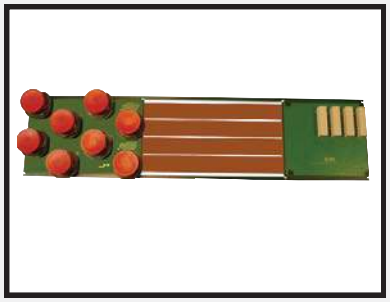
This machine is used to rework BGA and other fine-pitch components to ensure proper functionality and placement. The rework station's thermal, optical, and software features provide high reliability and ease of use together with the capability to handle the large assemblies (18" x 22") and wide range of components.

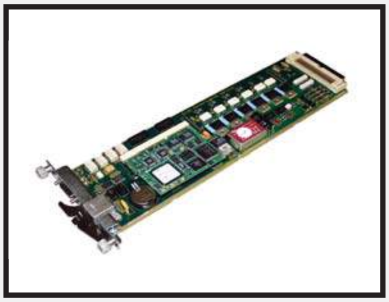
Carousel

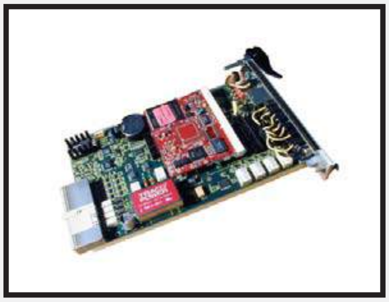
A vertical carousel is an automated storage and retrieval device consisting of a series of carriers (pans) mounted on a vertical closed-loop oval track, inside a metal enclosure. When activated, the pans rotate to bring requested items to the operator. The result is significant time and space savings, and a more accurate, efficient process

Elma Bustronic offers Contract Assembly services for various boards, adapters, monitors, and system accessories. From design services to boards assembly, Elma Bustronic can provide a solution for you.

Our assembly line includes a state-of-the-art Pick & Place machine which can support any components, from BGAs to items requiring the most accurate alignment. Details on our in-line printer, re-flow soldering system, and multi-solvent cleaner are available here http://www.elmabustronic.com/aassembly.htm The company also has a wide range of test & simulation equipment.



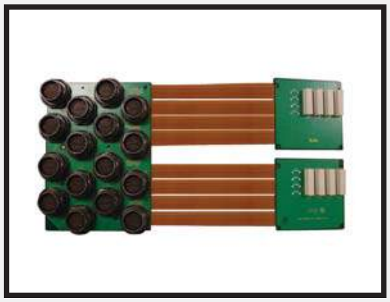


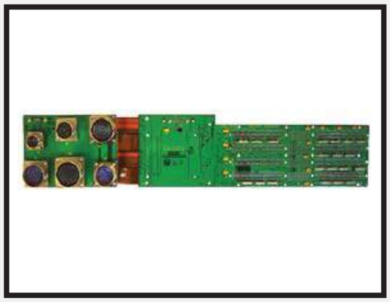


Rigid Flex Design

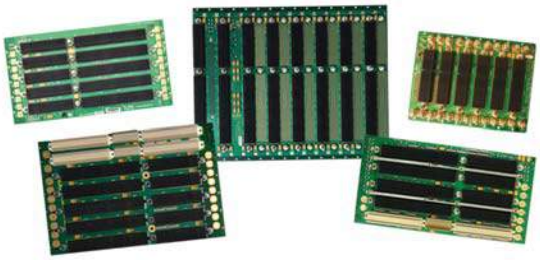
Elma Bustronic provides custom design and manufacturing solutions for rigid-flex backplanes. There are several special considerations for flex designs, including:

- Mechanical design – ensure flex is not strained or damaged. Careful that the flex does not bend sharply. The layers can bow and distort the reference plane.
- Routing – impedance changes from flex to rigid, etc. Consider signal integrity issues.
- Conformal coating process – proper coverlay for the polyimide material and masking for coating of the rigid part of the board.
- Layer analysis - optimize number of flex layers for maximum performance.







OpenVPX presents many design challenges and experienced teams like Elma Bustronic's are best suited to take them on. With 864 pins per slot carrying up to 192 differential pairs, there is an incredible amount of I/O to route through the backplane. Additionally, OpenVPX presently defines high-speed differential channels with bandwidths up to 6.25 Gbaud/s per lane. OpenVPX establishes specific requirements for slot, module and backplane profiles that standardize features and ensure system interoperability.

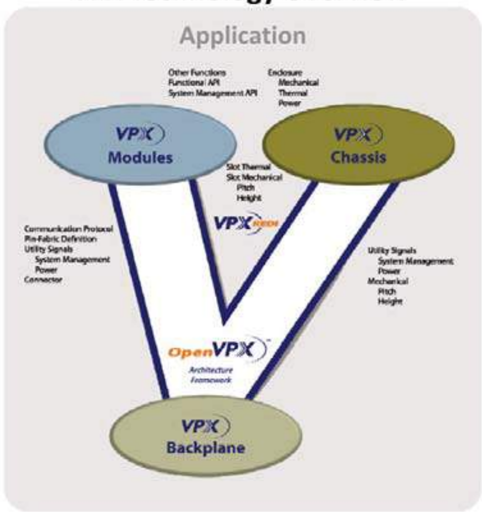
By preserving the VMEbus 6U mechanical form factor and through mapping of the current VMEbus signals to the MultiGig connectors, the OpenVPX technology brings several features to reality while maintaining ability to inter-operate with existing VME technology boards. VPX provides vastly increased high-speed serial I/O support for such needs as digital video, mass storage interconnects and FPGA interconnects. VPX also supports distributed switching that eliminates the need for dedicated switch card slots and allows for VITA 42 mezzanine sites with high speed I/O.

Elma Bustronic is the leader in VITA 46/65 VPX and OpenVPX products. Our experts developed the industry's first VPX backplane and proposed the first VME pinouts to the VITA 46 subcommittee. Since then, Elma has developed various VPX and OpenVPX configurations with and without legacy VME64x slots. VPX presents design challenges with higher layer-count backplanes, and more demanding power and cooling requirements. We tackle these problems with signal integrity analysis, thermal simulation and testing.

OpenVPX Background

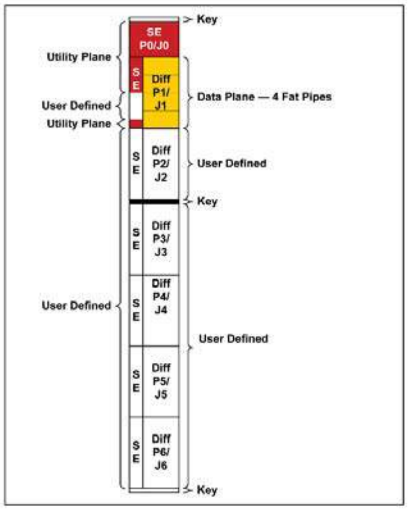
OpenVPX is an effort by a joint group of companies to provide definitions for system interoperability. VPX is a highly flexible architecture, allowing a wide range of configurations and topology options. OpenVPX provides an easier way to ensure interoperability between VPX systems. The VPX Modules and Slots across the backplanes have been given definitions so that similar Modules will work within certain Slot configurations. The backplane Configurations have been defined to show the collection of Slot profiles it entails, including information on the data rate, routing topology, and fabric used. Now, the integrator can determine that a daughter card Module from "X" company can be used in the same backplane slot as "Y" company's, when both Module Profiles specify the same Slot Profile.

VPX Technology Overview



VITA Based Backplanes

To explain OpenVPX, we'll use a 6U 5-slot Mesh OpenVPX backplane as an example. The diagram below shows the payload slot profile. It provides more information for the data plane section (in yellow), which in this case defines 4 fat pipe lanes. Also, the utility planes are clearly identified in red. Although this backplane does not have a control plane, if it had one, we'd also see this in the payload slot profile, along with the type of signal (thin pipes are commonly used for the control plane).



SLT6-PER-4F-10.3.1

The Slot Profile that is referenced in the two diagrams provide us some details on the card plugging into the slot. Going from the Slot profile number SLT6 says it's a 6U Slot profile (a 6U board), the PER says it's a Peripheral Slot, 4F means it has 4 fat pipes and the 10.3.1 is where you can find details on this slot profile in the VITA 65 specification. For OpenVPX, Fat Pipes have 4 links (4 Tx pairs + 4 Rx pairs), Thin Pipes have 2 links, and Ultra Thin pipes have one link. The wider channels like Fat Pipes are typically used in the data plane, while the control plane will often have the thin pipe or ultra thin-pipe signals. Slot types are comprised of Peripheral slots, Payload slots, Switch slots, or Bridge slots.

The Backplane Profile of the backplane also provides us more information. For example, this 6U 5-slot's profile is BKP6-DIS05-11.2.16-1. The BKP6 tells us it's a 6U backplane profile. DIS05 means it's a distributed (like a mesh or ring) architecture and has 5 slots. The 11.2.16 is the section of the specification where you can find details on this backplane profile. The "-1" tells us the Data rate is 3.125 Gbps (-2 means 5 Gbps and -3 means 6.250 Gbps)

The Backplane Profile Chart below shows the profile name, the pitch, the corresponding slot profile for the backplane, the control plane data rate (if applicable) and the data rate of the backplane.

	Mechanical		Slot Profiles and Section	Channel Gbaud Rate	
Profile name	Pitch (in)	RTM Conn	Payload	Control Plane	Data Plane
BKP6-DIS05-11.2.16-1	1.0	VITA 46.10	SLT6-PER-4F-10.3.1	1.25	3.125
BKP6-DIS05-11.2.16-2	1.0	VITA 46.10	SLT6-PER-4F-10.3.1	1.25	5.0
BKP6-DIS05-11.2.16-3	1.0	VITA 46.10	SLT6-PER-4F-10.3.1	1.25	6.25

Backplane Profile Chart

The slot type (like DIS05) section of the profile name is an important part of the description. The main fabric topologies are CEN for Centralized, DIS for Distributed, and HYB for Hybrid. "Centralized" means it has a centralized switch slot and the routing could be similar to a Star topology. The DIS and CEN configurations typically have Payload and Switch slot types. The HYB defines a Backplane Profile that typically will include a Bridge slot (such as, SLT6-BRG-4F1V2T-10.5-1). The Bridge slot is designed to accept an OpenVPX format front card that will serve as the interface to slots supporting slots utilizing a different connector system to support other Eurocard embedded architectures such as VME, CompactPCI™, or even CompactPCI Express™. Although only 6U BRG Slot Profiles and 6U HYB Backplane Profiles are currently defined within ANSI-VITA 65. 3U HYB Backplane Profiles and 3U BRG Slot Profiles are possible.

OpenVPX Backplanes

Height	Slots	Topology	Description	Profile	Corresponding Slot Profiles	Part Numbers
3U	3	Centralized	3U VITA 65, 3-slot, centralized switch, channel Gbaud rate up to 6.25	BKP3-CEN03-15.2.9-3	SLT3-PAY- 2F-14.2.7 SLT3-PER-1F-14.3.2	1OVX3031X6-1X11R 1OVX3031X6-1X10R
3U	5	Distributed	3U VITA 65, 5-slot with VITA 67 RF connectors on 3-slots, channel Gbaud rate up to 3.125	BKP3-DIS05-15.3.2-1	SLT3-SWH-4F-14.4.4 SLT3-PAY-4F4R-14.6.2	1OVX305DX1-1X11R 1OVX305DX1-1X10R
3U	6	Distributed	3U VITA 65, 6-slot VPX twisted ring with Ethernet control plane, channel Gbaud rate up to 6.25	BKP3-DIS06-15.2.14-3	SLT3-PAY-2F2T-14.2.5 SLT3-SWH-16T-14.4.6	1OVX306SX6-1X11R 1OVX306SX6-1X10R
3U	6	Distributed	3U VITA 65, 6-slot VPX twisted ring, channel Gbaud rate up to 6.25	BKP3-DIS06-15.2.7-3	SLT3-PAY-2F2T-14.2.5 SLT3-SWH-16T-14.4.6	1OVX306AX6-1X11R 1OVX306AX6-1X10R
3U	6	Centralized	VPX central switch with expansion plane, channel Gbaud rate up to 3.125	BKP3-CEN06-15.2.2-1	SLT3-PAY-1F2F2U-14.2.2 SLT3-SWH-6F6U-14.4.1	1OVX306UX1-1X11R 1OVX306UX1-1X10R
3U	6	Centralized	VPX central switch, payload in Slot 1 connected to slot 2, channel Gbaud rate up to 6.25	BKP3-CEN06-15.2.12-3	SLT3-PAY-2F-14.2.7 SLT3-SWH-4F-14.4.4 SLT3-PER-1F-14.3.2	1OVX306JX6-1X11R 1OVX306JX6-1X10R
3U	9	Distributed	3U VITA 65, 9-slot VPX central switch with and without expansion plane, channel Gbaud rate up to 6.25	BKP3-CEN09-15.2.17-3	SLT3-PAY-3F2U-14.2.13 SLT3-PAY-1F2U-14.2.12 SLT3-PAY-1F2F2U-14.2.2 SLT3-SWH-6F8U-14.4.9	1OVX309KX6-1X11R 1OVX309KX6-1X10R 1OVX309KY6-1X11R 1OVX309KY6-1X10R
6U	5	Distributed	6U VITA 65, 5-slot mesh, 4 lane fat pipe, channel Gbaud rate up to 6.25	BKP6-DIS05-11.2.16-3	SLT6-PER-4F-10.3.1	1OVX605MX6-1X01R 1OVX605MX6-1X00R
6U	5	Centralized	6U VITA 65, 5-slot, centralized switch, channel Gbaud rate up to 3.125	BKP6-CEN05-11.2.5-1	SLT6-PAY-4F1Q2U2T-10.2.1 SLT6-SWH-16U20F-10.4.2	1OVX605FX1-1X01R 1OVX605FX1-1X00R
6U	6	Distributed	6U VITA 65, 6-slot mesh with switch, channel Gbaud rate up to 6.25	BKP6-DIS06-11.2.10-3	SLT6-PAY-4F2T-10.2.2 SLT6-SWH-4F24T-10.4.4	1OVX606BX6-1X01R 1OVX606BX6-1X00R
6U	7	Hybrid	6U VITA 65, 7-slot (5 VPX + 2 legacy VME64x)	BKP6-HYB07-11.2.20-1	SLT6-BRG-4F1V2T-10.5.1 SLT6-PAY-4F2T-10.2.2 SLT6-SWH-4F24T-10.4.4	1OVX607EX1-1201R 1OVX607EX1-1200R
6U	9	Centralized	VPX central switch, channel Gbaud rate up to 3.125	BKP6-CEN09-11.2.13-1	SLT6-PAY-8F-10.2.3 SLT6-PER-2F-10.3.2	1OVX609VX1-1X01R 1OVX609VX1-1X00R
6U	10	Centralized	VPX Dual Star central switches with expansion and control planes, channel Gbaud rate up to 6.25	BKP6-CEN10-11.2.6-3	SLT6-PAY-4F1Q2U2T-10.2.1 SLT6-SWH-16U20F-10.4.2	1OVX610WX6-1X01R 1OVX610WX6-1X00R
6U	16	Centralized	VPX Dual Star central switches with expansion and control planes, channel Gbaud rate up to 6.25	BKP6-CEN16-11.2.2-3	SLT6-PAY-4F1Q2U2T-10.2.1 SLT6-SWH-20U19F-10.4.1	1OVX616GX6-1X01R 1OVX616GX6-1X00R
6U	17	Hybrid	6U VITA 65, 17-slot (14 VPX + 3 legacy VME64x)	BKP6-HYB17-11.2.11-1	SLT6-BRG-4F1V2T- 10.5.1 SLT6-PAY-4F2T-10.2.2 SLT6-SWH-4F24T-10.4.4	1OVX617NX1-1321R 1OVX617NX1-1320R

OpenVPX Accessories Overview

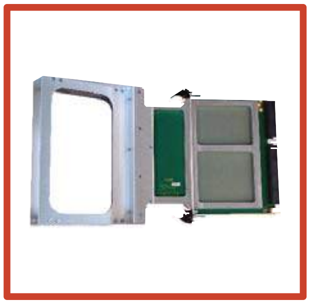
VPX Backplanes

Height	Slots	Topology	Description	Part Number
3U	1	n/a	3U VPX, 1-slot power and ground	101VPX301P-1X31R
3U	5	n/a	3U VPX, 5-slot power and ground	101VPX305P-1X31R
3U	6	n/a	3U VPX, 6-slot power and ground	101VPX306P-1X31R
7U	1	n/a	7U VPX, 1-slot power and ground	101VPX701P-1X40R
7U	1	n/a	7U VPX, 1-slot power and ground w/VITA 67 RF	1900002558-0000
7U	4	n/a	7U VPX, 4-slot power and ground	101VPX704P-1X40R*

* Consult factory for ordering details

Accessories

3U VPX Test Extender:
119EXT3024-07XX



6U VPX Test Extender:
119EXT6024-05XX

3U VPX Load Board, Conduction-Cooled:
1940000446-0000R

3U VPX Load Board, Convection-Cooled:
1940000345-0000R

6U VPX Load Board, Conduction-Cooled:
1940000376-0000R

6U VPX Load Board, Convection-Cooled:
1940000355-0000R

6U VPX RTM:
1940000352-0000R

SerDes Test Device, 16 channel w/ 2
VPX cables: 1940000511-0000

Features

- Compliant to ANSI/VITA 65-2010
- Compliant to the latest VITA 46 Specifications
- High-speed MultiGig connector
- Uses the rugged 3U-160 Eurocard form factor
- Centralized single star topology with one fat pipe to each slot
- Provides built in ESD ground protection in every slot

Mechanical Specifications

Height	Slots	Pitch
3U	3	1”

Multi-Gig RT-2 7-row connectors

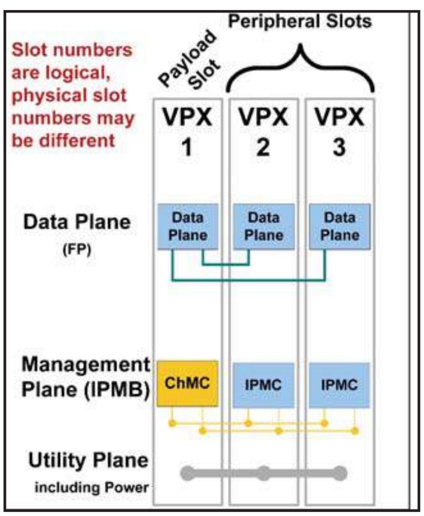
Board Specifications

Layers	2 oz. Copper Power & Ground	PCB FR-4 or Equivalent	PCB Thickness
14	Yes	Yes	.213”

The 3U, 3-slot OpenVPX backplane features one fat pipe routed to each slot in a single star topology. This leaves a wealth of User Defined pins in the P1 and P2 sections of the backplane.

See Signal Assignments and Backplane Profiles on page 25 and 34.

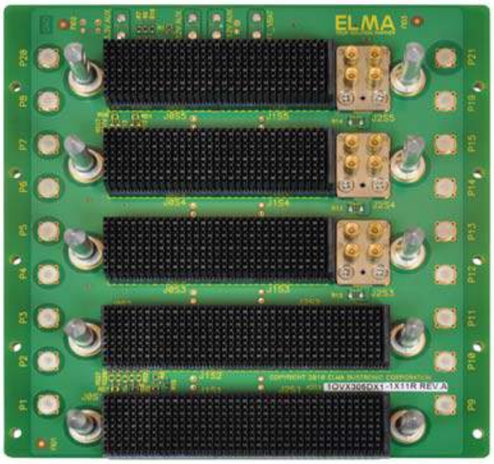
Backplane Topology



Order Information

Height	Slots	Description	Profile Number	Order Number
3U	3	3U VITA 65, VPX central switch, up to 6.25 Gbaud channel data rate	BKP3-CEN03-15.2.9-3	1OVX303QX6-1X11R
3U	3	3U VITA 65, VPX central switch, up to 6.25 Gbaud channel data rate, no RTM connectors	BKP3-CEN03-15.2.9-3	1OVX303QX6-1X10R

OpenVPX Backplanes - 3U, 5-Slot



Features

- Compliant to ANSI/VITA 65-2010
- Compliant to the latest VITA 46 Specifications
- A 4-cavity RF connector installed in 3 slots of the lower half of the standard J2 connector. This corresponds to rows 9-16 of slots 3, 4 and 5
- High-speed MultiGig connector
- Uses the rugged 3U-160 Eurocard form factor
- Mesh routing topology with all four fat pipes connected across all slots
- Provides built in ESD ground protection in every slot

Mechanical Specifications

Height	Slots	Pitch
3U	5	1.0”

Multi-Gig RT-2 7-row connectors

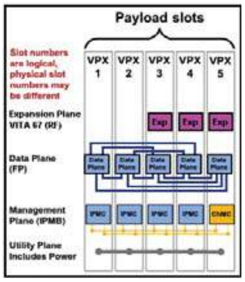
Board Specifications

Layers	2 oz. Copper Power & Ground	PCB FR-4 or Equivalent	PCB Thickness
14	Yes	Yes	.213”

The 3U, 5-slot OpenVPX backplane has 3 slots for VITA 67 RF connectors, which are passthrough only. Otherwise, the design incorporates a distributed mesh topology.

See Signal Assignments and Backplane Profiles on page 25 and 34.

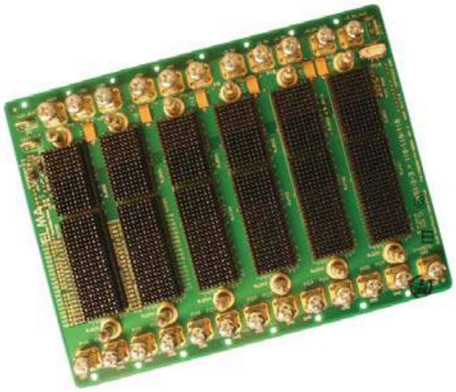
Backplane Topology



Order Information

Height	Slots	Description	Profile Number	Order Number
3U	5	Mesh with 3 VITA 67 RF connector interfaces	BKP3-DIS05-15.3.2-1	1OVX305DX1-1X11R
3U	5	Mesh with 3 VITA 67 RF connector interfaces, no RTM connectors	BKP3-DIS05-15.3.2-1	1OVX305DX1-1X10R

OpenVPX Backplanes - 3U, 6-Slot



Features

- Compliant to ANSI/VITA 65-2010
- Compliant to the latest VITA 46 Specifications
- High-speed MultiGig connector
- Uses the rugged 3U-160 Eurocard form factor
- Channels A and B are arranged as 2 fat pipes (x4) channels configured as a twisted ring extending from slots 1 to 5
- Provides built in ESD ground protection in every slot
- Versions with or without GigE Control Plane
- Version with slot 6 not connected to other slots for use with RTM

Mechanical Specifications

Height	Slots	Pitch
3U	6	1.0”

Multi-Gig RT-2 7-row connectors

Board Specifications

Layers	2 oz. Copper Power & Ground	PCB FR-4 or Equivalent	PCB Thickness
22 SX, AX & JX version 16 UX version	Yes	Yes	.212” SX, AX & JX version .173” UX version

Utilizing a twisted-ring topology versus a mesh topology allows for more I/O pins and ability to use mezzanines like XMC. A full mesh topology over 3U VPX would simply take up the vast majority of available pins. In the Elma Bustronic 3U VPX backplane (twisted ring versions), slot 6 has configurable thin pipe links for distributed Gigabit Ethernet to slot 1 through slot 5 and two fat pipes for rear I/O. In slots 1-5 any or all of the P1 thin pipes (x2 channels) assigned to the control channel star can be reconfigured as rear I/O by removing zero ohm SMT shunts. In slots 1-5 all P2 differential pairs are available on the rear side for I/O. In the “AX” part number version, slot 6 is not connected to the other slots, allowing undefined pins for an RTM slot. The only defined pins to the RTM are the 2x thin pipes for the control plane.

The VPX Gigabit Ethernet Control Plane adds a GigE switch, providing a separate star or dual star network for out-of-band communication. This can be particularly important for system management, software and firmware upgrades, and initiating new processes on specific boards.

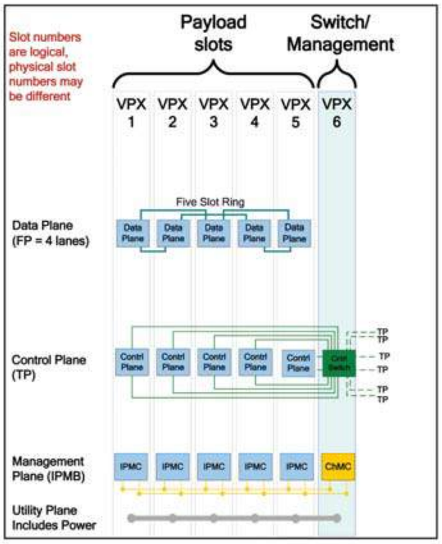
The Elma Bustronic design solution offers 3.125 to 6.250Gbauds/performance in in one PCB. This design provides maximum performance while saving you money. The central switch version of our 3U, 6-slot OpenVPX backplane features a fat pipe expansion plane, a fat pipe Star topology data plane, and an ultra thin pipe for the control plane. It is designed using Nelco-13SI PCB material.

See Signal Assignments and Backplane Profiles on page 26-27 and 34-35.

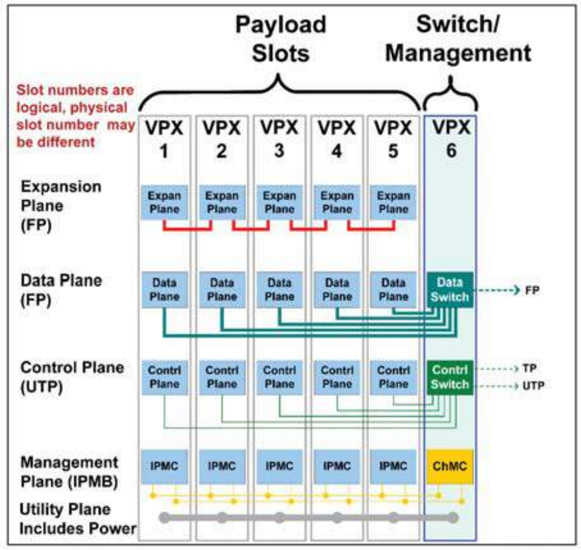
Order Information

Height	Slots	Description	Profile Number	Order Number
3U	6	VPX twisted ring with configurable Ethernet Control Plane, channel Gbaud rate up to 6.25	BKP3-DIS06-15.2.14-3	1OVX306SX6-1X11R
3U	6	VPX twisted ring with configurable Ethernet Control Plane, channel Gbaud rate up to 6.25, no RTM connectors	BKP3-DIS06-15.2.14-3	1OVX306SX6-1X10R
3U	6	VPX twisted ring, channel Gbaud rate up to 6.25	BKP3-DIS06-15.2.7-3	1OVX306AX6-1X11R
3U	6	VPX twisted ring, channel Gbaud rate up to 6.25, no RTM connectors	BKP3-DIS06-15.2.7-3	1OVX306AX6-1X10R
3U	6	VPX central switch with expansion plane	BKP3-CEN06-15.2.2-1	1OVX306UX1-1X11R
3U	6	VPX central switch with expansion plane, no RTM connectors	BKP3-CEN06-15.2.2-1	1OVX306UX1-1X10R
3U	6	VPX central switch, payload in Slot 1 connected to slot 2, channel Gbaud rate up to 6.25	BKP3-CEN06-15.2.12-3	1OVX306JX6-1X11R
3U	6	VPX central switch, payload in Slot 1 connected to slot 2, channel Gbaud rate up to 6.25, no RTM connectors	BKP3-CEN06-15.2.12-3	1OVX306JX6-1X10R

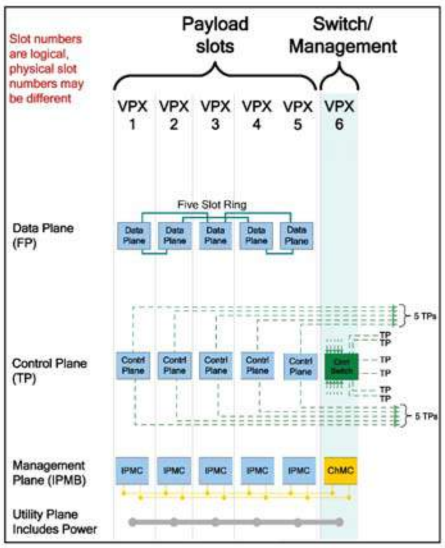
Backplane Topology



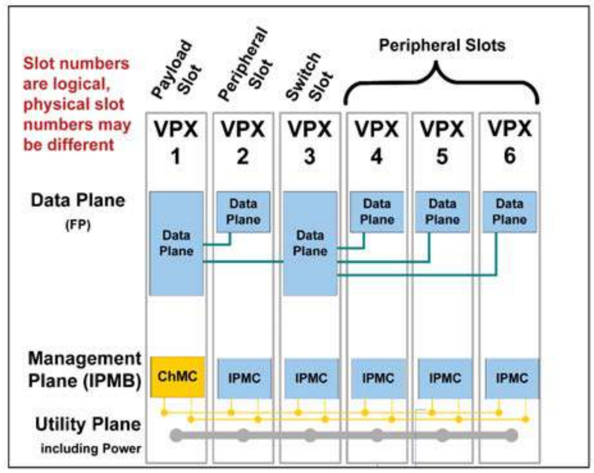
BKP3-DIS06-15.2.14



BKP3-CEN06-15.2.2

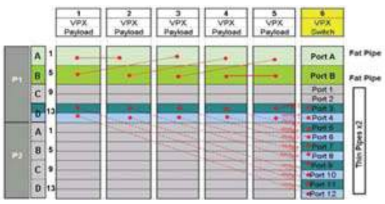


BKP3-DIS06-15.2.7

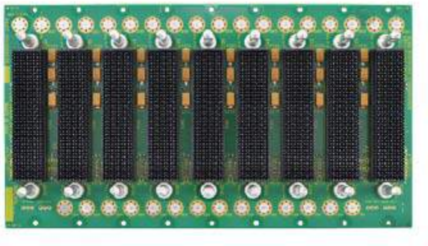


BKP3-CEN06-15.2.12

Port Mapping



Ports A and B in slots 1-5 are fat pipes implemented via one twisted ring as the primary VITA 46 fabric. The fabric may be 10G Ethernet (10GBASE KX-4), sRIO, or PCIe. Slot 6 is a switch slot for a thin pipe, redundant dual star, or distributed GigE. The GigE is configurable at each of the slots 1-5 so that any individual slot could utilize ports in J1 rows 9-12 for rear I/O if desired. Port A and port B in slot 6 have 10G Ethernet rear I/O.



Features
- Version with expansion plane compliant to VITA 65 specification. Version without expansion plane is VITA 65 compatible.
- Uses the rugged 3U-160 Eurocard form factor
- High-speed MultiGig connector
- Version with expansion plane in slots 5-8
- Provides built in ESD ground protection in every slot

Mechanical Specifications

Height	Slots
3U	9

Multi-Gig RT-2 7-row connectors

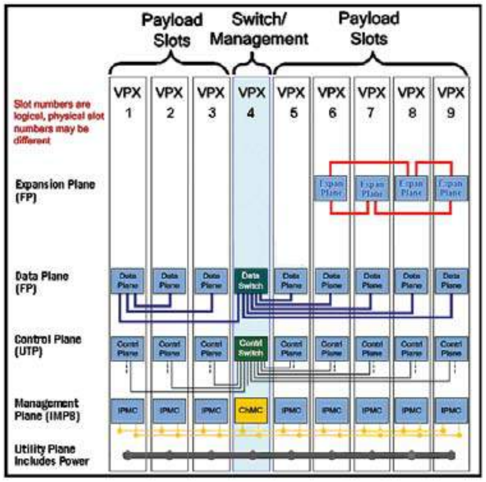
Board Specifications

Layers	2 oz. Copper Power & Ground	PCB FR-4 or Equivalent	PCB Thickness
16 KX version 18 KY version	Yes	Yes	.213"

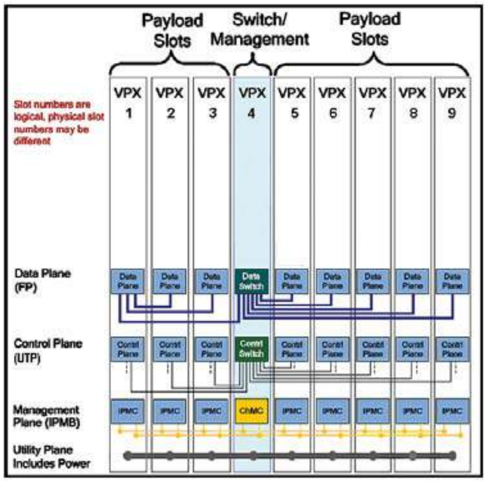
Elma Bustronic offers two versions of the BKP3-CEN09-15.2.17-n backplane: one with an expansion control plane and one without. Designed to VITA 65 design principles, the 9-slot OpenVPX backplane features a centralized routing topology. The switch slot is connected to slots 1, 5, 6, 7, 8, and 9. Slots 1-3 are also connected on the data plane. The version with the expansion plane have those signals going across slots 6-9. Contiguous groups of slots can have their maskable reset pin joined via jumpers within a provided backplane header.

See Signal Assignments and Backplane Profiles on page 27 and 35.

3U, 9-Slot with Expansion Plane Backplane Topology



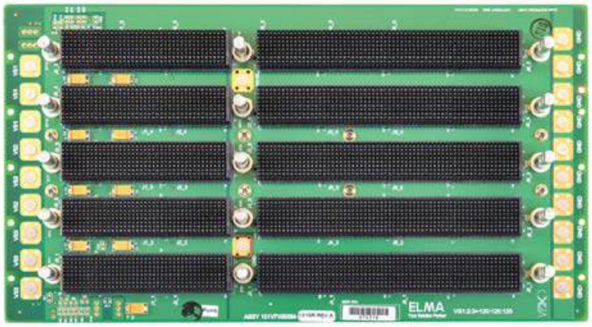
3U, 9-Slot without Expansion Plane Backplane Topology



Order Information

Height	Slots	Description	Profile Number	Order Number
3U	9	VPX central switch with expansion plane, channel Gbaud rate up to 6.25	BKP3-CEN09-15.2-17-3	1OVX309KX6-1X11R
3U	9	VPX central switch with expansion plane, channel Gbaud rate up to 6.25, no RTM connectors	BKP3-CEN09-15.2-17-3	1OVX309KX6-1X10R
3U	9	VPX central switch without expansion plane, channel Gbaud rate up to 6.25	BKP3-CEN09-15.2-17-3	1OVX309KY6-1X11R
3U	9	VPX central switch without expansion plane, no RTM connectors, channel Gbaud rate up to 6.25	BKP3-CEN09-15.2-17-3	1OVX309KY6-1X10R

OpenVPX Backplanes - 6U, 5 and 6-Slot



5 & 6-Slot Mesh Backplane Features

- Compliant to ANSI/VITA 65-2010
- Compliant to the latest VITA 46 Specifications
- High-speed Multi-gig connector
- Rugged Eurocard form factor in 6U height
- Provides built in ESD ground protection in every slot
- Signal integrity analysis report available upon request
- Distributed and centralized topology versions available

Mechanical Specifications

Height	Slots	Pitch
6U	5, 6	1.0”

Multi-Gig RT-2 7-row connectors

Board Specifications

Slots	Layers	2 oz. Copper Power & Ground	PCB FR-4 or Equivalent	PCB Thickness
5	18	Yes	Yes	.212”
6	16	Yes	Yes	.212”

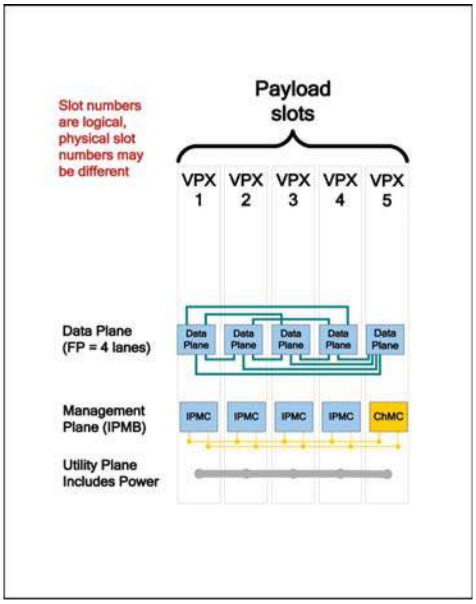
Elma Bustronic’s 6U OpenVPX backplanes come in centralized and distributed topologies. The centralized version features a double fat pipe expansion plane and a dual star routing topology for the data plane. The distributed topologies offer 3.125 to 6.250 Gbauds/performance in one PCB. This design provides maximum performance while saving you money.

See Signal Assignments and Backplane Profiles on page 28-29 and 35-36.

Order Information

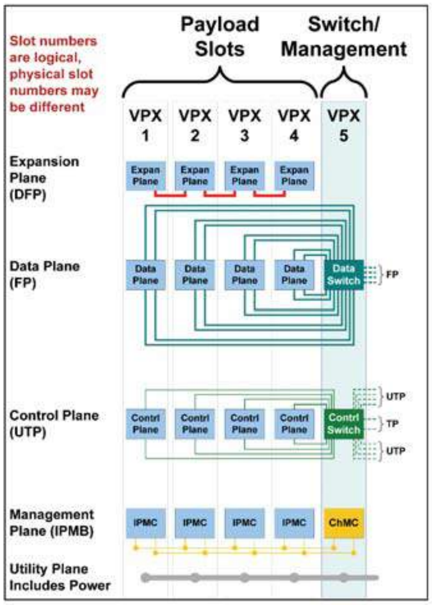
Height	Slots	Description	Profile Number	Order Number
6U	5	VPX central switch, channel Gbaud rate up to 3.125	BKP6-CEN05-11.2.5-1	1OVX605FX1-1X01R
6U	5	VPX central switch, channel Gbaud rate up to 3.125, no RTM connectors	BKP6-CEN05-11.2.5-1	1OVX605FX1-1X00R
6U	5	VPX mesh, 4 lane fat pipe, up to 6.25 Gbps per channel	BKP6-DIS05-11.2.16-3	1OVX605MX6-1X01R
6U	5	VPX mesh, 4 lane fat pipe up to 6.25 Gbps per channel, no RTM connectors	BKP6-DIS05-11.2.16-3	1OVX605MX6-1X00R
6U	6	VPX mesh data plane with switched control plane, up to 6.25 Gbaud channel data rate	BKP6-DIS06-11.2.10-3	1OVX606BX6-1X01R
6U	6	VPX mesh data plane with switched control plane, up to 6.25 Gbaud channel data rate, no RTM connectors	BKP6-DIS06-11.2.10-3	1OVX606BX6-1X00R

6U, 5-Slot Backplane Topology



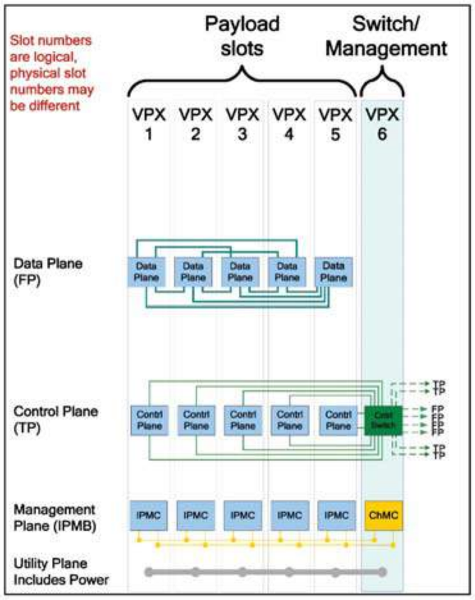
BKP6-DIS05-11.2.16

6U, 5-Slot Backplane Topology



BKP6-CEN05-11.2.5

6U, 6-Slot Backplane Topology



BKP6-DIS06-11.2.10

OpenVPX Backplanes - 6U, 9-Slot

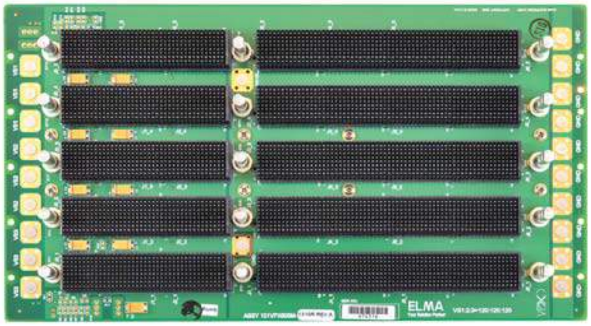


Photo of 5-slot version shown

Features

- Compliant to ANSI/VITA 65-2010
- Compliant to the latest VITA 46 Specifications
- High-speed Multi-gig connector
- Rugged Eurocard form factor in 6U height
- Provides built in ESD ground protection in every slot
- Signal integrity analysis report available upon request

Mechanical Specifications

Height	Slots	Pitch
6U	9	1.0"

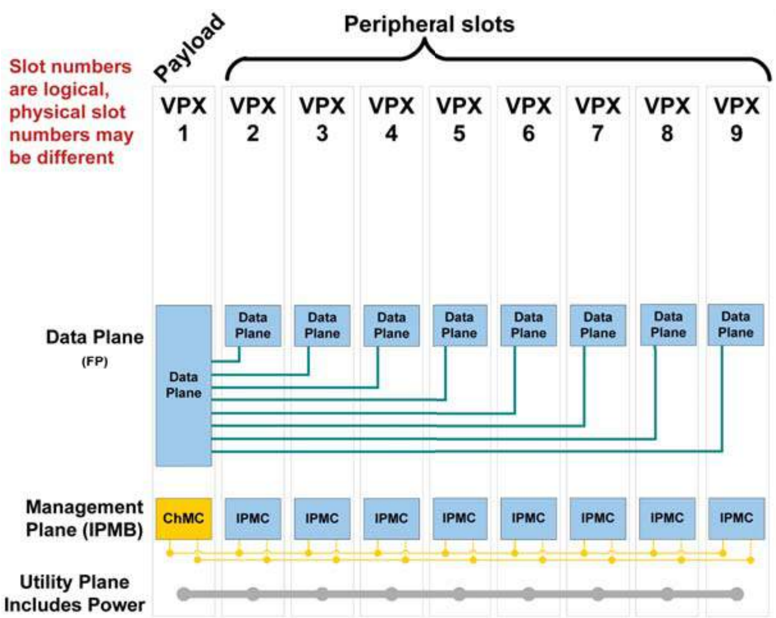
Multi-Gig RT-2 7-row connectors

Board Specifications

Slots	Layers	2 oz. Copper Power & Ground	PCB FR-4 or Equivalent	PCB Thickness
9	TBD	Yes	Yes	TBD

The Elma Bustronic BKP6-CEN09-11.2.13-1 6U OpenVPX backplane comes in a Star central slot topology with fat pipes routed to each slot.

See Signal Assignments and Backplane Profiles on page 30 and 36.



Order Information

Height	Slots	Description	Profile Number	Order Number
6U	9	VPX central switch, channel Gbaud rate up to 3.125	BKP6-CEN09-11.2.13-1	1OVX609VX1-1X01R
6U	9	VPX central switch, channel Gbaud rate up to 3.125, no RTM connectors	BKP6-CEN09-11.2.13-1	1OVX609VX1-1X00R

OpenVPX Backplanes - 6U, 10-Slot

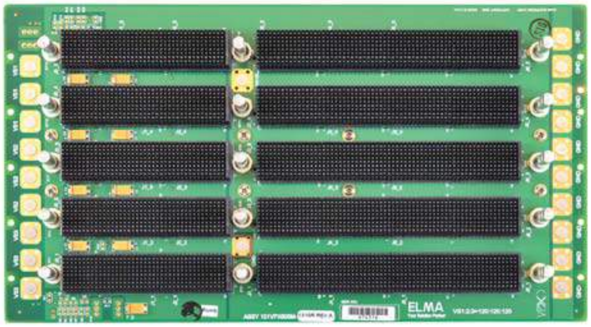


Photo of 5-slot version shown

Features

- Compliant to ANSI/VITA 65-2010
- Compliant to the latest VITA 46 Specifications
- Dual Star routing topology
- High-speed Multi-gig connector
- Rugged Eurocard form factor in 6U height
- Provides built in ESD ground protection in every slot
- Signal integrity analysis report available upon request

Mechanical Specifications

Height	Slots
6U	10

Multi-Gig RT-2 7-row connectors

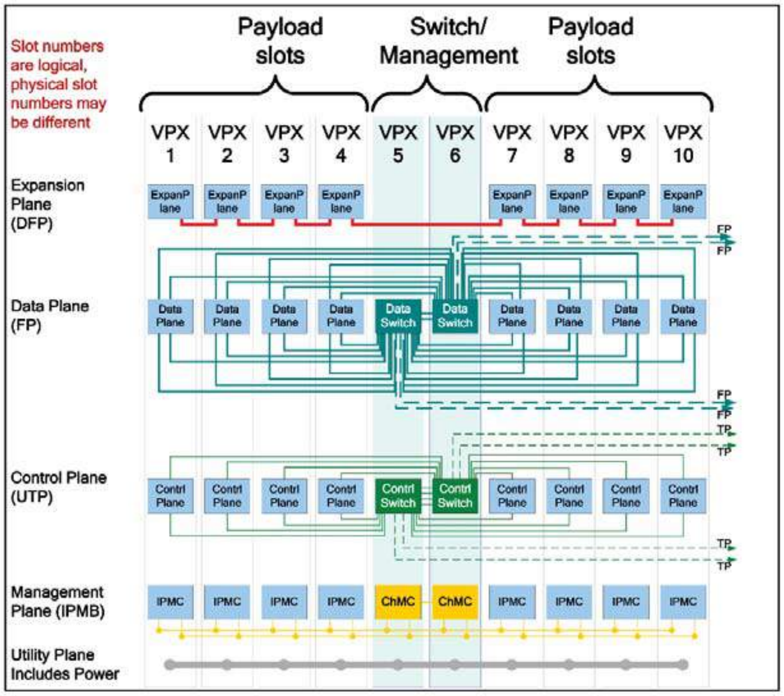
Board Specifications

Layers	2 oz. Copper Power & Ground	PCB FR-4 or Equivalent	PCB Thickness
TBD	Yes	Yes	TBD

The Elma Bustronic BKP6-CEN10-11.2.6-3 6U OpenVPX backplane comes in a Dual Star centralized routing topology with two switch slots with fat pipes to each slots. The control plane is also a Dual Star topology with ultra thin pipes to each slots. The expansion plane is a direct connection of all of the payload slots in a double fat pipe topology. The data plane has fat pipes available and the control plane has thin pipes that can be assessed from an RTM or via cables.

The backplane offers 3.125 to 6.250 Gbauds/performance in one PCB. This design provides maximum performance while saving you money.

See Signal Assignments and Backplane Profiles on page 31 and 36.



Order Information

Height	Slots	Description	Profile Number	Order Number
6U	10	VPX Dual Star central switches with expansion and control planes, channel Gbaud rate up to 6.25	BKP6-CEN10-11.2.6-3	1OVX610WX6-1X11R
6U	10	VPX Dual Star central switches with expansion and control planes, channel Gbaud rate up to 6.25, no RTM connectors	BKP6-CEN10-11.2.6-3	1OVX610WX6-1X10R

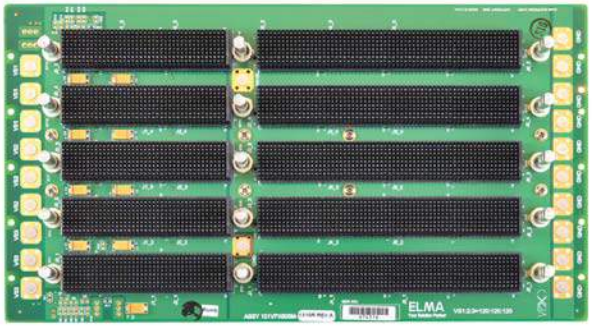


Photo of 5-slot version shown

Features

- Compliant to ANSI/VITA 65-2010
- Compliant to the latest VITA 46 Specifications
- High-speed Multi-gig connector
- Rugged Eurocard form factor in 6U height
- Provides built in ESD ground protection in every slot
- Signal integrity analysis report available upon request

Mechanical Specifications

Height	Slots	Pitch
6U	16	1.0”

Multi-Gig RT-2 7-row connectors

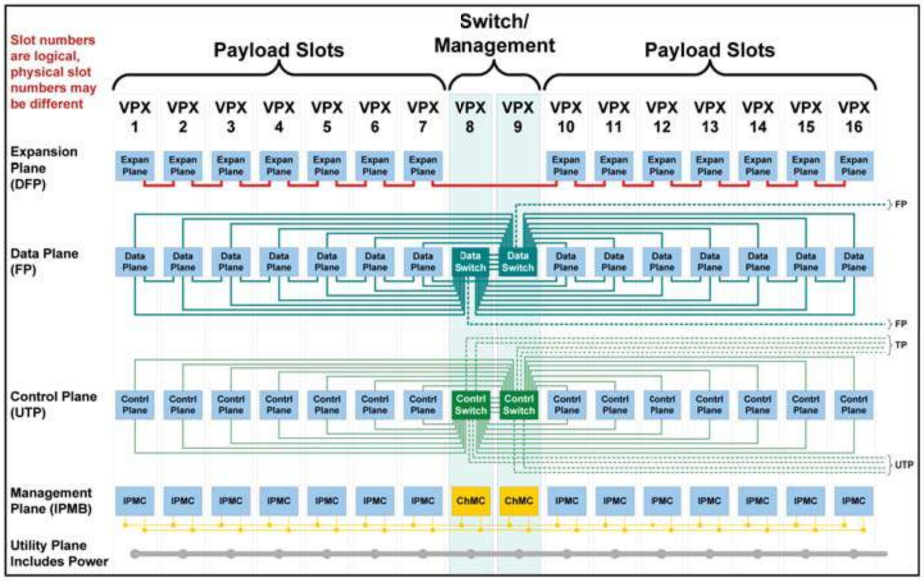
Board Specifications

Slots	Layers	2 oz. Copper Power & Ground	PCB FR-4 or Equivalent	PCB Thickness
16	28	Yes	Yes	.213”

The Elma Bustronic BKP6-CEN16-11.2.2-3 6U OpenVPX backplane comes in a Dual Star centralized routing topology with two switch slots with fat pipes to each slots. The control plane is also a Dual Star topology with ultra thin pipes to each slots. The expansion plane is a direct connection of all of the payload slots in a double fat pipe topology. The data plane has fat pipes available and the control plane has thin pipes and ultra thin pipes that can be assessed from an RTM or via cables.

The backplane offers 3.125 to 6.250 Gbauds/performance in one PCB. This design provides maximum performance while saving you money.

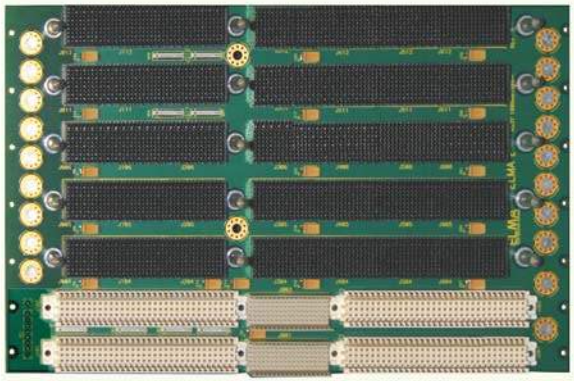
See Signal Assignments and Backplane Profiles on page 32 and 37.



Order Information

Height	Slots	Description	Profile Number	Order Number
6U	16	VPX Dual Star central switches with expansion and control planes, channel Gbaud rate up to 6.25	BKP6-CEN16-11.2.2-3	1OVX616GX6-1X01R
6U	16	VPX Dual Star central switches with expansion and control planes, channel Gbaud rate up to 6.25, no RTM connectors	BKP6-CEN16-11.2.2-3	1OVX616GX6-1X00R

OpenVPX Backplanes - 6U Hybrid



FEATURES
- Compliant to ANSI/VITA 65-2010
- Compliant to the latest VITA 46 Specifications
- Offers a highly flexible interconnect scheme that can support either differential or single ended connection
- Hybrid VPX backplane with legacy VME64x slots
- Rugged Eurocard form factor in 6U height
- Provides built in ESD ground protection in every slot

Mechanical Specifications

Height	Slots	Pitch
6U	7 slots (5 VPX, 2 VME64x)	1.0”
6U	17 slots (14 VPX, 3 VME64x)	1.0”

Multi-Gig RT-2 7-row connectors

Board Specifications

Slots	Layers	2 oz. Copper Power & Ground	PCB FR-4 or Equivalent	PCB Thickness
7	16	Yes	Yes	.213”
17	18	Yes	Yes	.213”

OpenVPX can be compatible with legacy systems in “hybrid” backplanes. The VMEbus signals can go across the MultiGig high-speed connectors to the legacy VME/64x slots.

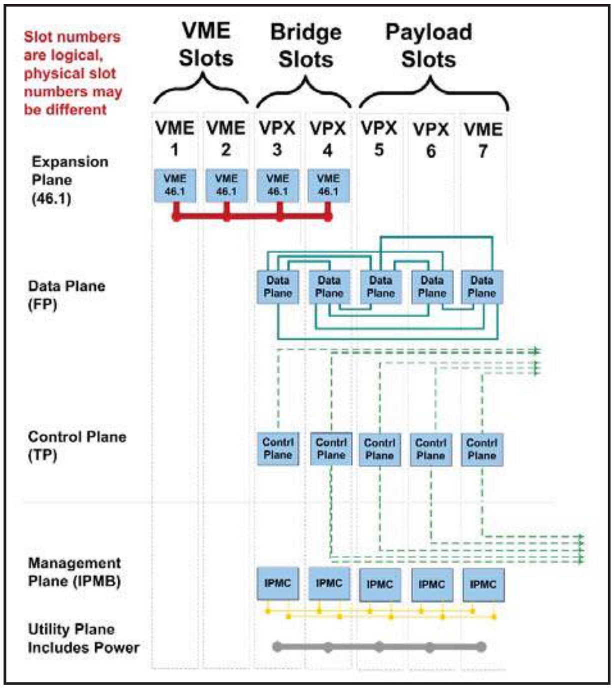
The 7 slot (5 VPX slots + 2 legacy VME64x slots) has a slot pitch of 0.8” in slots 1 -2 and 1.0” for the 5 VPX slots 3-7. Slots 3-4 have VME bussing on the J2 connector per VITA 46.1 and slots 3-7 have a full mesh implemented on the J1 connector. VPX slots 3-7 conform to IEEE 1101.10 and VITA 46.0, 46.3 and 46.10 as well as 46.1 where specified to be fully meshed with four fabric channels – one channel from each slot to each of the other four slots. The flexible design offers a combination of VME/64x only, VPX w/VME bussed slots, meshed VPX slots, and VPX-only slots.

See Signal Assignments and Backplane Profiles on page 30 (7-slot), 33 (17-slot) and 36 (7-slot), 37 (17-slot).

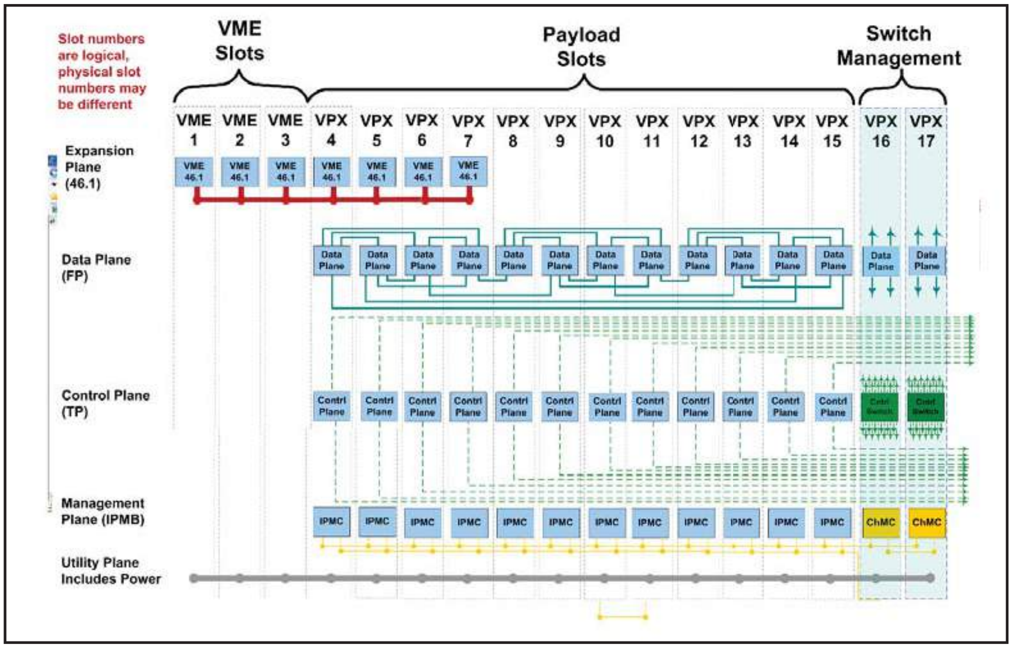
Order Information

Height	Slots	Description	Profile Number	Order Number
6U	7	5 VPX mesh slots with 2 legacy VME64x	BKP6-HYB07-11.2.20-1	1OVX607EX1-1201R
6U	7	5 VPX mesh slots with 2 legacy VME64x, no RTM connectors	BKP6-HYB07-11.2.20-1	1OVX607EX1-1200R
6U	17	17 slots (14 VPX + 3 legacy VME64x) of 4 slots and 2 end VPX slots are configurable 3 VPX mesh clusters	BKP6-HYB17-11.2.11-1	1OVX617NX1-1301R
6U	17	17 slots (14 VPX + 3 legacy VME64x) of 4 slots and 2 end VPX slots are configurable 3 VPX mesh clusters, no RTM connectors	BKP6-HYB17-11.2.11-1	1OVX617NX1-1300R

6U, 7-Slot Backplane Topology



6U, 17-Slot Backplane Topology



Order Information

1OVX ☐☐☐☐☐☐ - ☐☐☐☐☐

Product Type

OVX = OpenVPX compatible

☐ Height

3 = 3U
6 = 6U
7 = 7U

☐☐ Slots

02-20

☐☐ Slots

MX = BKP6-DIS05-11.2.16
SX = BKP3-DIS06-15.2.14
DX = BKP3-DIS05-15.3.1
NX = BKP6-HYB17-11.2.11
AX = BKP3-DIS06-15.2.7
BX = BKP6-DIS06-11.2.10
EX = BKP6-HYB07-11.2.20
KX = BKP3-CEN09-15.2-17
KY = BKP3-CEN09-15.2-17
QX = BKP3-CEN03-15.2.9
FX = BKP6-CEN05-11.2.5
UX = BKP3-CEN06-15.2.2
GX = BKP6-CEN16-11.2.2
JX = BKP3-DIS06-15.2.12
VX = BKP6-CEN09-11.2.13
WX = BKP6-CEN10-11.2.6

☐ Data Rate

1 = Data plane 3.125 Gbaud
2 = Data plane 5.0 Gbaud
3 = Data plane 6.25 Gbaud
4 = Data plane 10 Gbaud
5 = Not used, for future use
6 = Data plane up to 6.25 Gbaud (same cost-effective PCB used for 3.125 to 6.25 versions)

☐ Power Interface

1 = 8/32 threaded stud

☐ Hybrid

1 = 1 VME64X slot
2 = 2 VME64X slot
3 = 3 VME64X slot
4 = 4 VME64X slot
5 = 5 VME64X slot
6 = 6 VME64X slot
X = not applicable

☐ Voltage

0 = 5V, 12V (6U ONLY) AND -12V AUX, +12V AUX, 3.3V AUX
1 = 3.3V, 5V, 12V (3U ONLY) AND -12V AUX, +12V AUX, 3.3V AUX
2 = 3U/6U power

☐ Rear I/O

0 = No rear I/O connectors
1 = As required by VITA 65, refer to RTM connector configuration

☐ RoHS

R = RoHS compliant
S = RoHS 5/6 compliant
(Blank) = not RoHS compliant

3U, 3-Slot Signal Assignments

J0 Signal Assignments

	Row I	Row H	Row G	Row F	Row E	Row D	Row C	Row B	Row A
1	Vs1	Vs1	Vs1	Vs1	No Pad	Vs2	Vs2	Vs2	Vs2
2	Vs1	Vs1	Vs1	Vs1	No Pad	Vs2	Vs2	Vs2	Vs2
3	Vs3	Vs3	Vs3	Vs3	No Pad	Vs3	Vs3	Vs3	Vs3
4	GND	SM2	SM3	GND	-12V_Aux	GND	SYSRESET*	NVMRO	GND
5	GND	GAP*	GA4*	GND	3.3V_Aux	GND	SM0	SM1	GND
6	GND	GA3*	GA2*	GND	+12V_Aux	GND	GA1*	GA0*	GND
7	TCK	GND	GND	TDO	TDI	GND	GND	TMS	TRST*
8	GND	REF_CLK-	REF_CLK+	GND	GND	AUX_CLK-	AUX_CLK+	GND	GND

J1 Payload Signal Assignments

Plug-In Module P1		Row G	Row F	Row E Even	Row E Odd	Row D	Row C	Row B Even	Row B Odd	Row A
Bplane J1		Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a
1	Data Plane Port 1	GDiscrete1	GND	GND-J1	DP01-T0-	DP01-T0+	GND	GND-J1	DP01-R0-	DP01-R0+
2	Data Plane Port 1	GND	DP01-T1-	DP01-T1+	GND-J1	GND	DP01-R1-	DP01-R1+	GND-J1	GND
3	Data Plane Port 1	P1-VBAT	GND	GND-J1	DP01-T2-	DP01-T2+	GND	GND-J1	DP01-R2-	DP01-R2+
4	Data Plane Port 1	GND	DP01-T3-	DP01-T3+	GND-J1	GND	DP01-R3-	DP01-R3+	GND-J1	GND
5	Data Plane Port 2	SYS_CON*	GND	GND-J1	DP02-T0-	DP02-T0+	GND	GND-J1	DP02-R0-	DP02-R0+
6	Data Plane Port 2	GND	DP02-T1-	DP02-T1+	GND-J1	GND	DP02-R1-	DP02-R1+	GND-J1	GND
7	Data Plane Port 2	Reserved	GND	GND-J1	DP02-T2-	DP02-T2+	GND	GND-J1	DP02-R2-	DP02-R2+
8	Data Plane Port 2	GND	DP02-T3-	DP02-T3+	GND-J1	GND	DP02-R3-	DP02-R3+	GND-J1	GND
9	User defined	UD	GND	GND-J1	UD	UD	GND	GND-J1	UD	UD
10	User defined	GND	UD	UD	GND-J1	GND	UD	UD	GND-J1	GND
11	User defined	UD	GND	GND-J1	UD	UD	GND	GND-J1	UD	UD
12	User defined	GND	UD	UD	GND-J1	GND	UD	UD	GND-J1	GND
13	User defined	UD	GND	GND-J1	UD	UD	GND	GND-J1	UD	UD
14	User defined	GND	UD	UD	GND-J1	GND	UD	UD	GND-J1	GND
15	User defined	Maskable Reset*	GND	GND-J1	UD	UD	GND	GND-J1	UD	UD
16	User defined	GND	UD	UD	GND-J1	GND	UD	UD	GND-J1	GND

J1 Peripheral Signal Assignments

Plug-In Module P1		Row G	Row F	Row E Even	Row E Odd	Row D	Row C	Row B Even	Row B Odd	Row A
Bplane J1		Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a
1	Data Plane Port 1	GDiscrete1	GND	GND-J1	DP01-T0-	DP01-T0+	GND	GND-J1	DP01-R0-	DP01-R0+
2	Data Plane Port 1	GND	DP01-T1-	DP01-T1+	GND-J1	GND	DP01-R1-	DP01-R1+	GND-J1	GND
3	Data Plane Port 1	P1-VBAT	GND	GND-J1	DP01-T2-	DP01-T2+	GND	GND-J1	DP01-R2-	DP01-R2+
4	Data Plane Port 1	GND	DP01-T3-	DP01-T3+	GND-J1	GND	DP01-R3-	DP01-R3+	GND-J1	GND
5	User defined	SYS_CON*	GND	GND-J1	UD	UD	GND	GND-J1	UD	UD
6	User defined	GND	UD	UD	GND-J1	GND	UD	UD	GND-J1	GND
7	User defined	Reserved	GND	GND-J1	UD	UD	GND	GND-J1	UD	UD
8	User defined	GND	UD	UD	GND-J1	GND	UD	UD	GND-J1	GND
9	User defined	UD	GND	GND-J1	UD	UD	GND	GND-J1	UD	UD
10	User defined	GND	UD	UD	GND-J1	GND	UD	UD	GND-J1	GND
11	User defined	UD	GND	GND-J1	UD	UD	GND	GND-J1	UD	UD
12	User defined	GND	UD	UD	GND-J1	GND	UD	UD	GND-J1	GND
13	User defined	UD	GND	GND-J1	UD	UD	GND	GND-J1	UD	UD
14	User defined	GND	UD	UD	GND-J1	GND	UD	UD	GND-J1	GND
15	User defined	Maskable Reset*	GND	GND-J1	UD	UD	GND	GND-J1	UD	UD
16	User defined	GND	UD	UD	GND-J1	GND	UD	UD	GND-J1	GND

3U, 5-Slot Signal Assignments

J0 Signal Assignments

	Row I	Row H	Row G	Row F	Row E	Row D	Row C	Row B	Row A
1	Vs1	Vs1	Vs1	Vs1	No Pad	Vs2	Vs2	Vs2	Vs2
2	Vs1	Vs1	Vs1	Vs1	No Pad	Vs2	Vs2	Vs2	Vs2
3	Vs3	Vs3	Vs3	Vs3	No Pad	Vs3	Vs3	Vs3	Vs3
4	GND	SM2	SM3	GND	-12V_Aux	GND	SYSRESET*	NVMRO	GND
5	GND	GAP*	GA4*	GND	3.3V_Aux	GND	SM0	SM1	GND
6	GND	GA3*	GA2*	GND	+12V_Aux	GND	GA1*	GA0*	GND
7	TCK	GND	GND	TDO	TDI	GND	GND	TMS	TRST*
8	GND	REF_CLK-	REF_CLK+	GND	GND	AUX_CLK-	AUX_CLK+	GND	GND

J1 Signal Assignments

Plug-In Module P1		Row G	Row F	Row E Even	Row E Odd	Row D	Row C	Row B Even	Row B Odd	Row A
Bplane J1		Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a
1	Data Plane Port 1	GDiscrete1	GND	GND-J1	DP01-T0-	DP01-T0+	GND	GND-J1	DP01-R0-	DP01-R0+
2	Data Plane Port 1	GND	DP01-T1-	DP01-T1+	GND-J1	GND	DP01-R1-	DP01-R1+	GND-J1	GND
3	Data Plane Port 1	P1-VBAT	GND	GND-J1	DP01-T2-	DP01-T2+	GND	GND-J1	DP01-R2-	DP01-R2+
4	Data Plane Port 1	GND	DP01-T3-	DP01-T3+	GND-J1	GND	DP01-R3-	DP01-R3+	GND-J1	GND
5	Data Plane Port 2	SYS_CON*	GND	GND-J1	DP02-T0-	DP02-T0+	GND	GND-J1	DP02-R0-	DP02-R0+
6	Data Plane Port 2	GND	DP02-T1-	DP02-T1+	GND-J1	GND	DP02-R1-	DP02-R1+	GND-J1	GND
7	Data Plane Port 2	Reserved	GND	GND-J1	DP02-T2-	DP02-T2+	GND	GND-J1	DP02-R2-	DP02-R2+
8	Data Plane Port 2	GND	DP02-T3-	DP02-T3+	GND-J1	GND	DP02-R3-	DP02-R3+	GND-J1	GND
9	Data Plane Port 3	UD	GND	GND-J1	DP03-T0-	DP03-T0+	GND	GND-J1	DP03-R0-	DP03-R0+
10	Data Plane Port 3	GND	DP03-T1-	DP03-T1+	GND-J1	GND	DP03-R1-	DP03-R1+	GND-J1	GND
11	Data Plane Port 3	UD	GND	GND-J1	DP03-T2-	DP03-T2+	GND	GND-J1	DP03-R2-	DP03-R2+
12	Data Plane Port 3	GND	DP03-T3-	DP03-T3+	GND-J1	GND	DP03-R3-	DP03-R3+	GND-J1	GND
13	Data Plane Port 4	UD	GND	GND-J1	DP04-T0-	DP04-T0+	GND	GND-J1	DP04-R0-	DP04-R0+
14	Data Plane Port 4	GND	DP04-T1-	DP04-T1+	GND-J1	GND	DP04-R1-	DP04-R1+	GND-J1	GND
15	Data Plane Port 4	Maskable Reset*	GND	GND-J1	DP04-T2-	DP04-T2+	GND	GND-J1	DP04-R2-	DP04-R2+
16	Data Plane Port 4	GND	DP04-T3-	DP04-T3+	GND-J1	GND	DP04-R3-	DP04-R3+	GND-J1	GND

J2/P2 Signal Assignments* (Slots 1-2)

Plug In Module P2~P6				Row G	Row F	Row E Even	Row E Odd	Row D	Row C	Row B Even	Row B Odd	Row A
Backplane J2~J6				Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a
1	X16 using [15:0]	x8 using [7:0]	x4 using [3:0]	SEwafer1	GND	GND-J2	LN0-TD-	LN0-TD+	GND	GND-J2	LN0-RD-	LN0-RD+
2	X16 using [15:0]	x8 using [7:0]	x4 using [3:0]	GND	LN1-TD-	LN1-TD+	GND-J2	GND	LN1-RD-	LN1-RD+	GND-J2	GND
3	X16 using [15:0]	x8 using [7:0]	x4 using [3:0]	SEwafer3	GND	GND-J2	LN2-TD-	LN2-TD+	GND	GND-J2	LN2-RD-	LN2-RD+
4	X16 using [15:0]	x8 using [7:0]	x4 using [3:0]	GND	LN3-TD-	LN3-TD+	GND-J2	GND	LN3-RD-	LN3-RD+	GND-J2	GND
5	X16 using [15:0]	x8 using [7:0]	x4 using [7:4]	SEwafer5	GND	GND-J2	LN4-TD-	LN4-TD+	GND	GND-J2	LN4-RD-	LN4-RD+
6	X16 using [15:0]	x8 using [7:0]	x4 using [7:4]	GND	LN5-TD-	LN5-TD+	GND-J2	GND	LN5-RD-	LN5-RD+	GND-J2	GND
7	X16 using [15:0]	x8 using [7:0]	x4 using [7:4]	SEwafer7	GND	GND-J2	LN6-TD-	LN6-TD+	GND	GND-J2	LN6-RD-	LN6-RD+
8	X16 using [15:0]	x8 using [7:0]	x4 using [7:4]	GND	LN7-TD-	LN7-TD+	GND-J2	GND	LN7-RD-	LN7-RD+	GND-J2	GND
9	X16 using [15:0]	x8 using [15:8]	x4 using [11:8]	SEwafer9	GND	GND-J2	LN8-TD-	LN8-TD+	GND	GND-J2	LN8-RD-	LN8-RD+
10	X16 using [15:0]	x8 using [15:8]	x4 using [11:8]	GND	LN9-TD-	LN9-TD+	GND-J2	GND	LN9-RD-	LN9-RD+	GND-J2	GND
11	X16 using [15:0]	x8 using [15:8]	x4 using [11:8]	SEwafer11	GND	GND-J2	LN10-TD-	LN10-TD+	GND	GND-J2	LN10-RD-	LN10-RD+
12	X16 using [15:0]	x8 using [15:8]	x4 using [11:8]	GND	LN11-TD-	LN11-TD+	GND-J2	GND	LN11-RD-	LN11-RD+	GND-J2	GND
13	X16 using [15:0]	x8 using [15:8]	x4 using [15:12]	SEwafer13	GND	GND-J2	LN12-TD-	LN12-TD+	GND	GND-J2	LN12-RD-	LN12-RD+
14	X16 using [15:0]	x8 using [15:8]	x4 using [15:12]	GND	LN13-TD-	LN13-TD+	GND-J2	GND	LN13-RD-	LN13-RD+	GND-J2	GND
15	X16 using [15:0]	x8 using [15:8]	x4 using [15:12]	SEwafer15	GND	GND-J2	LN14-TD-	LN14-TD+	GND	GND-J2	LN14-RD-	LN14-RD+
16	X16 using [15:0]	x8 using [15:8]	x4 using [15:12]	GND	LN15-TD-	LN15-TD+	GND-J2	GND	LN15-RD-	LN15-RD+	GND-J2	GND

* Any signal pins pass through the rear

J2/P2 Signal Assignments (Slots 3-5)

Plug In Module P2~P6				Row G	Row F	Row E Even	Row E Odd	Row D	Row C	Row B Even	Row B Odd	Row A
Backplane J2~J6				Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a
1		x8 using [7:0]	x4 using [3:0]	SEwafer1	GND	GND-J2	LN0-TD-	LN0-TD+	GND	GND-J2	LN0-RD-	LN0-RD+
2		x8 using [7:0]	x4 using [3:0]	GND	LN1-TD-	LN1-TD+	GND-J2	GND	LN1-RD-	LN1-RD+	GND-J2	GND
3		x8 using [7:0]	x4 using [3:0]	SEwafer3	GND	GND-J2	LN2-TD-	LN2-TD+	GND	GND-J2	LN2-RD-	LN2-RD+
4		x8 using [7:0]	x4 using [3:0]	GND	LN3-TD-	LN3-TD+	GND-J2	GND	LN3-RD-	LN3-RD+	GND-J2	GND
5		x8 using [7:0]	x4 using [7:4]	SEwafer5	GND	GND-J2	LN4-TD-	LN4-TD+	GND	GND-J2	LN4-RD-	LN4-RD+
6		x8 using [7:0]	x4 using [7:4]	GND	LN5-TD-	LN5-TD+	GND-J2	GND	LN5-RD-	LN5-RD+	GND-J2	GND
7		x8 using [7:0]	x4 using [7:4]	SEwafer7	GND	GND-J2	LN6-TD-	LN6-TD+	GND	GND-J2	LN6-RD-	LN6-RD+
8		x8 using [7:0]	x4 using [7:4]	GND	LN7-TD-	LN7-TD+	GND-J2	GND	LN7-RD-	LN7-RD+	GND-J2	GND

VITA Based Backplanes

OpenVPX Backplanes - Signal Assignments

3U, 6-Slot Signal Assignments (BKP3-DIS06-15-2.14, BKP3-DIS06-15.2.7)

J0 Signal Assignments

	Row I	Row H	Row G	Row F	Row E	Row D	Row C	Row B	Row A
1	Vs1	Vs1	Vs1	Vs1	No Pad	Vs2	Vs2	Vs2	Vs2
2	Vs1	Vs1	Vs1	Vs1	No Pad	Vs2	Vs2	Vs2	Vs2
3	Vs3	Vs3	Vs3	Vs3	No Pad	Vs3	Vs3	Vs3	Vs3
4	GND	SM2	SM3	GND	-12V_Aux	GND	SYSRESET*	NVMRO	GND
5	GND	GAP*	GA4*	GND	3.3V_Aux	GND	SM0	SM1	GND
6	GND	GA3*	GA2*	GND	+12V_Aux	GND	GA1*	GA0*	GND
7	TCK	GND	GND	TDO	TDI	GND	GND	TMS	TRST*
8	GND	REF_CLK-	REF_CLK+	GND	GND	AUX_CLK-	AUX_CLK+	GND	GND

J1 Payload Signal Assignments

Plug-In Module P1		Row G	Row F	Row E Even	Row E Odd	Row D	Row C	Row B Even	Row B Odd	Row A
Backplane J1		Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a
1	Data Plane Port 1 x4/ 2x2/ 1x4 X8	GDiscrete1	GND	GND-J1	DP01-TD0-	DP01-TD0+	GND	GND-J1	DP01-RD0-	DP01-RD0+
2		GND	DP01-TD1-	DP01-TD1+	GND-J1	GND	DP01-RD1-	DP01-RD1+	GND-J1	GND
3		P1-VBAT	GND	GND-J1	DP01-TD2-	DP01-TD2+	GND	GND-J1	DP01-RD2-	DP01-RD2+
4		GND	DP01-TD3-	DP01-TD3+	GND-J1	GND	DP01-RD3-	DP01-RD3+	GND-J1	GND
5	Data Plane Port 2 x4/ 2x2/ 1x4	SYS_CON*	GND	GND-J1	DP02-TD0-	DP02-TD0+	GND	GND-J1	DP02-RD0-	DP02-RD0+
6		GND	DP02-TD1-	DP02-TD1+	GND-J1	GND	DP02-RD1-	DP02-RD1+	GND-J1	GND
7		Reserved	GND	GND-J1	DP02-TD2-	DP02-TD2+	GND	GND-J1	DP02-RD2-	DP02-RD2+
8		GND	DP02-TD3-	DP02-TD3+	GND-J1	GND	DP02-RD3-	DP02-RD3+	GND-J1	GND
9	User Defined	UD	GND	GND-J1	UD	UD	GND	GND-J1	UD	UD
10		GND	UD	UD	GND-J1	GND	UD	UD	GND-J1	GND
11		UD	GND	GND-J1	UD	UD	GND	GND-J1	UD	UD
12		GND	UD	UD	GND-J1	GND	UD	UD	GND-J1	GND
13	Control Plane	UD	GND	GND-J4	CPtp02-DB-	CPtp02-DB+	GND	GND-J4	CPtp02-DA-	CPtp02-DA+
14		GND	CPtp02-DD-	CPtp02-DD+	GND-J4	GND	CPtp02-DC-	CPtp02-DC+	GND-J4	GND
15		Maskable Reset*	GND	GND-J4	CPtp01-DB-	CPtp01-DB+	GND	GND-J4	CPtp01-DA-	CPtp01-DA+
16		GND	CPtp01-DD-	CPtp01-DD+	GND-J4	GND	CPtp01-DC-	CPtp01-DC+	GND-J4	GND

J1 Switch Signal Assignments

Plug-In Module P1		Row G	Row F	Row E Even	Row E Odd	Row D	Row C	Row B Even	Row B Odd	Row A
Backplane J1		Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a
1	Control Plane Port 1	GDiscrete1	GND	GND-J1	CP01-T0-	CP01-T0+	GND	GND-J1	CP01-R0-	CP01-R0+
2		GND	CP01-T1-	CP01-T1+	GND-J1	GND	CP01-R1-	CP01-R1+	GND-J1	GND
3		P1-VBAT	GND	GND-J1	CP01-T2-	CP01-T2+	GND	GND-J1	CP01-R2-	CP01-R2+
4		GND	CP01-T3-	CP01-T3+	GND-J1	GND	CP01-R3-	CP01-R3+	GND-J1	GND
5	Control Plane Port 2	SYS_CON*	GND	GND-J1	CP02-T0-	CP02-T0+	GND	GND-J1	CP02-R0-	CP02-R0+
6		GND	CP02-T1-	CP02-T1+	GND-J1	GND	CP02-R1-	CP02-R1+	GND-J1	GND
7		Reserved	GND	GND-J1	CP02-T2-	CP02-T2+	GND	GND-J1	CP02-R2-	CP02-R2+
8		GND	CP02-T3-	CP02-T3+	GND-J1	GND	CP02-R3-	CP02-R3+	GND-J1	GND
9	Control Plane Ports 1 - 8	UD	GND	GND-J1	CPutp01-TD-	CPutp01-TD+	GND	GND-J1	CPutp01-RD-	CPutp01-RD+
10		GND	CPutp02-TD-	CPutp02-TD+	GND-J1	GND	CPutp02-RD-	CPutp02-RD+	GND-J1	GND
11		UD	GND	GND-J1	CPutp03-TD-	CPutp03-TD+	GND	GND-J1	CPutp03-RD-	CPutp03-RD+
12		GND	CPutp04-TD-	CPutp04-TD+	GND-J1	GND	CPutp04-RD-	CPutp04-RD+	GND-J1	GND
13		UD	GND	GND-J1	CPutp05-TD-	CPutp05-TD+	GND	GND-J1	CPutp05-RD-	CPutp05-RD+
14		GND	CPutp06-TD-	CPutp06-TD+	GND-J1	GND	CPutp06-RD-	CPutp06-RD+	GND-J1	GND
15		Maskable Reset*	GND	GND-J1	CPutp07-TD-	CPutp07-TD+	GND	GND-J1	CPutp07-RD-	CPutp07-RD+
16		GND	CPutp08-TD-	CPutp08-TD+	GND-J1	GND	CPutp08-RD-	CPutp08-RD+	GND-J1	GND

J2/P2 Signal Assignments* (Slots 1-5)

Plug inModule P2~P6		Row G	Row F	Row E Even	Row E Odd	Row D	Row C	Row B Even	Row B Odd	Row A
Backplane J2~J6		Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a
1	X16 using [15:0]	SEwafer1	GND	GND-J2	LN0-TD-	LN0-TD+	GND	GND-J2	LN0-RD-	LN0-RD+
2		GND	LN1-TD-	LN1-TD+	GND-J2	GND	LN1-RD-	LN1-RD+	GND-J2	GND
3		SEwafer3	GND	GND-J2	LN2-TD-	LN2-TD+	GND	GND-J2	LN2-RD-	LN2-RD+
4		GND	LN3-TD-	LN3-TD+	GND-J2	GND	LN3-RD-	LN3-RD+	GND-J2	GND
5		SEwafer5	GND	GND-J2	LN4-TD-	LN4-TD+	GND	GND-J2	LN4-RD-	LN4-RD+
6		GND	LN5-TD-	LN5-TD+	GND-J2	GND	LN5-RD-	LN5-RD+	GND-J2	GND
7		SEwafer7	GND	GND-J2	LN6-TD-	LN6-TD+	GND	GND-J2	LN6-RD-	LN6-RD+
8		GND	LN7-TD-	LN7-TD+	GND-J2	GND	LN7-RD-	LN7-RD+	GND-J2	GND
9		SEwafer9	GND	GND-J2	LN8-TD-	LN8-TD+	GND	GND-J2	LN8-RD-	LN8-RD+
10		GND	LN9-TD-	LN9-TD+	GND-J2	GND	LN9-RD-	LN9-RD+	GND-J2	GND
11		SEwafer11	GND	GND-J2	LN10-TD-	LN10-TD+	GND	GND-J2	LN10-RD-	LN10-RD+
12		GND	LN11-TD-	LN11-TD+	GND-J2	GND	LN11-RD-	LN11-RD+	GND-J2	GND
13		SEwafer13	GND	GND-J2	LN12-TD-	LN12-TD+	GND	GND-J2	LN12-RD-	LN12-RD+
14		GND	LN13-TD-	LN13-TD+	GND-J2	GND	LN13-RD-	LN13-RD+	GND-J2	GND
15		SEwafer15	GND	GND-J2	LN14-TD-	LN14-TD+	GND	GND-J2	LN14-RD-	LN14-RD+
16		GND	LN15-TD-	LN15-TD+	GND-J2	GND	LN15-RD-	LN15-RD+	GND-J2	GND

* Any signal pins pass through the rear

J2/P2 Switch Signal Assignments (Slot 6)

Plug-In Module P2		Row G	Row F	Row E Even	Row E Odd	Row D	Row C	Row B Even	Row B Odd	Row A
Backplane J2		Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a
1	Control Plane Port 9 - 24	UD	GND	GND-J2	CPutp09-TD-	CPutp09-TD+	GND	GND-J2	CPutp09-RD-	CPutp09-RD+
2		GND	CPutp10-TD-	CPutp10-TD+	GND-J2	GND	CPutp10-RD-	CPutp10-RD+	GND-J2	GND
3		UD	GND	GND-J2	CPutp11-TD-	CPutp11-TD+	GND	GND-J2	CPutp11-RD-	CPutp11-RD+
4		GND	CPutp12-TD-	CPutp12-TD+	GND-J2	GND	CPutp12-RD-	CPutp12-RD+	GND-J2	GND
5		UD	GND	GND-J2	CPutp13-TD-	CPutp13-TD+	GND	GND-J2	CPutp13-RD-	CPutp13-RD+
6		GND	CPutp14-TD-	CPutp14-TD+	GND-J2	GND	CPutp14-RD-	CPutp14-RD+	GND-J2	GND
7		UD	GND	GND-J2	CPutp15-TD-	CPutp15-TD+	GND	GND-J2	CPutp15-RD-	CPutp15-RD+
8		GND	CPutp16-TD-	CPutp16-TD+	GND-J2	GND	CPutp16-RD-	CPutp16-RD+	GND-J2	GND
9		UD	GND	GND-J2	CPutp17-TD-	CPutp17-TD+	GND	GND-J2	CPutp17-RD-	CPutp17-RD+
10		GND	CPutp18-TD-	CPutp18-TD+	GND-J2	GND	CPutp18-RD-	CPutp18-RD+	GND-J2	GND
11		UD	GND	GND-J2	CPutp19-TD-	CPutp19-TD+	GND	GND-J2	CPutp19-RD-	CPutp19-RD+
12		GND	CPutp20-TD-	CPutp20-TD+	GND-J2	GND	CPutp20-RD-	CPutp20-RD+	GND-J2	GND
13		UD	GND	GND-J2	CPutp21-TD-	CPutp21-TD+	GND	GND-J2	CPutp21-RD-	CPutp21-RD+
14		GND	CPutp22-TD-	CPutp22-TD+	GND-J2	GND	CPutp22-RD-	CPutp22-RD+	GND-J2	GND
15		UD	GND	GND-J2	CPutp23-TD-	CPutp23-TD+	GND	GND-J2	CPutp23-RD-	CPutp23-RD+
16		GND	CPutp24-TD-	CPutp24-TD+	GND-J2	GND	CPutp24-RD-	CPutp24-RD+	GND-J2	GND

3U, 6-Slot Signal Assignments (BKP3-CEN06-15.2.12)

J0 Signal Assignments

	Row I	Row H	Row G	Row F	Row E	Row D	Row C	Row B	Row A
1	Vs1	Vs1	Vs1	Vs1	No Pad	Vs2	Vs2	Vs2	Vs2
2	Vs1	Vs1	Vs1	Vs1	No Pad	Vs2	Vs2	Vs2	Vs2
3	Vs3	Vs3	Vs3	Vs3	No Pad	Vs3	Vs3	Vs3	Vs3
4	GND	SM2	SM3	GND	-12V_Aux	GND	SYSRESET*	NVMRO	GND
5	GND	GAP*	GA4*	GND	3.3V_Aux	GND	SM0	SM1	GND
6	GND	GA3*	GA2*	GND	+12V_Aux	GND	GA1*	GA0*	GND
7	TCK	GND	GND	TDO	TDI	GND	GND	TMS	TRST*
8	GND	REF_CLK-	REF_CLK+	GND	GND	AUX_CLK-	AUX_CLK+	GND	GND

J1/P1 Payload Signal Assignments

Plug-In Module P1		Row G	Row F	Row E Even	Row E Odd	Row D	Row C	Row B Even	Row B Odd	Row A
Bplane J1		Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a
1	Data Plane Port 1	GDiscrete1	GND	GND-J1	DP01-T0-	DP01-T0+	GND	GND-J1	DP01-R0-	DP01-R0+
2		GND	DP01-T1-	DP01-T1+	GND-J1	GND	DP01-R1-	DP01-R1+	GND-J1	GND
3		P1-VBAT	GND	GND-J1	DP01-T2-	DP01-T2+	GND	GND-J1	DP01-R2-	DP01-R2+
4		GND	DP01-T3-	DP01-T3+	GND-J1	GND	DP01-R3-	DP01-R3+	GND-J1	GND
5	Data Plane Port 2	SYS_CON*	GND	GND-J1	DP02-T0-	DP02-T0+	GND	GND-J1	DP02-R0-	DP02-R0+
6		GND	DP02-T1-	DP02-T1+	GND-J1	GND	DP02-R1-	DP02-R1+	GND-J1	GND
7		Reserved	GND	GND-J1	DP02-T2-	DP02-T2+	GND	GND-J1	DP02-R2-	DP02-R2+
8		GND	DP02-T3-	DP02-T3+	GND-J1	GND	DP02-R3-	DP02-R3+	GND-J1	GND
9	User defined	UD	GND	GND-J1	UD	UD	GND	GND-J1	UD	UD
10		GND	UD	UD	GND-J1	GND	UD	UD	GND-J1	GND
11		UD	GND	GND-J1	UD	UD	GND	GND-J1	UD	UD
12		GND	UD	UD	GND-J1	GND	UD	UD	GND-J1	GND
13		UD	GND	GND-J1	UD	UD	GND	GND-J1	UD	UD
14		GND	UD	UD	GND-J1	GND	UD	UD	GND-J1	GND
15		Maskable Reset*	GND	GND-J1	UD	UD	GND	GND-J1	UD	UD
16		GND	UD	UD	GND-J1	GND	UD	UD	GND-J1	GND

J1/P1 Switch Signal Assignments

Plug-In Module P1		Row G	Row F	Row E Even	Row E Odd	Row D	Row C	Row B Even	Row B Odd	Row A
Bplane J1		Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a
1	Data Plane Port 1	GDiscrete1	GND	GND-J1	DP01-T0-	DP01-T0+	GND	GND-J1	DP01-R0-	DP01-R0+
2		GND	DP01-T1-	DP01-T1+	GND-J1	GND	DP01-R1-	DP01-R1+	GND-J1	GND
3		P1-VBAT	GND	GND-J1	DP01-T2-	DP01-T2+	GND	GND-J1	DP01-R2-	DP01-R2+
4		GND	DP01-T3-	DP01-T3+	GND-J1	GND	DP01-R3-	DP01-R3+	GND-J1	GND
5	Data Plane Port 2	SYS_CON*	GND	GND-J1	DP02-T0-	DP02-T0+	GND	GND-J1	DP02-R0-	DP02-R0+
6		GND	DP02-T1-	DP02-T1+	GND-J1	GND	DP02-R1-	DP02-R1+	GND-J1	GND
7		Reserved	GND	GND-J1	DP02-T2-	DP02-T2+	GND	GND-J1	DP02-R2-	DP02-R2+
8		GND	DP02-T3-	DP02-T3+	GND-J1	GND	DP02-R3-	DP02-R3+	GND-J1	GND
9	Data Plane Port 3	UD	GND	GND-J1	DP03-T0-	DP03-T0+	GND	GND-J1	DP03-R0-	DP03-R0+
10		GND	DP03-T1-	DP03-T1+	GND-J1	GND	DP03-R1-	DP03-R1+	GND-J1	GND
11		UD	GND	GND-J1	DP03-T2-	DP03-T2+	GND	GND-J1	DP03-R2-	DP03-R2+
12		GND	DP03-T3-	DP03-T3+	GND-J1	GND	DP03-R3-	DP03-R3+	GND-J1	GND
13	Data Plane Port 4	UD	GND	GND-J1	DP04-T0-	DP04-T0+	GND	GND-J1	DP04-R0-	DP04-R0+
14		GND	DP04-T1-	DP04-T1+	GND-J1	GND	DP04-R1-	DP04-R1+	GND-J1	GND
15		Maskable Reset*	GND	GND-J1	DP04-T2-	DP04-T2+	GND	GND-J1	DP04-R2-	DP04-R2+
16		GND	DP04-T3-	DP04-T3+	GND-J1	GND	DP04-R3-	DP04-R3+	GND-J1	GND

J1/P1 Peripheral Signal Assignments

Plug-In Module P1		Row G	Row F	Row E Even	Row E Odd	Row D	Row C	Row B Even	Row B Odd	Row A
Bplane J1		Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a
1	Data Plane Port 1	GDiscrete1	GND	GND-J1	DP01-T0-	DP01-T0+	GND	GND-J1	DP01-R0-	DP01-R0+
2		GND	DP01-T1-	DP01-T1+	GND-J1	GND	DP01-R1-	DP01-R1+	GND-J1	GND
3		P1-VBAT	GND	GND-J1	DP01-T2-	DP01-T2+	GND	GND-J1	DP01-R2-	DP01-R2+
4		GND	DP01-T3-	DP01-T3+	GND-J1	GND	DP01-R3-	DP01-R3+	GND-J1	GND
5	User defined	SYS_CON*	GND	GND-J1	UD	UD	GND	GND-J1	UD	UD
6		GND	UD	UD	GND-J1	GND	UD	UD	GND-J1	GND
7		Reserved	GND	GND-J1	UD	UD	GND	GND-J1	UD	UD
8		GND	UD	UD	GND-J1	GND	UD	UD	GND-J1	GND
9		UD	GND	GND-J1	UD	UD	GND	GND-J1	UD	UD
10		GND	UD	UD	GND-J1	GND	UD	UD	GND-J1	GND
11		UD	GND	GND-J1	UD	UD	GND	GND-J1	UD	UD
12		GND	UD	UD	GND-J1	GND	UD	UD	GND-J1	GND
13		UD	GND	GND-J1	UD	UD	GND	GND-J1	UD	UD
14		GND	UD	UD	GND-J1	GND	UD	UD	GND-J1	GND
15		Maskable Reset*	GND	GND-J1	UD	UD	GND	GND-J1	UD	UD
16		GND	UD	UD	GND-J1	GND	UD	UD	GND-J1	GND

All J2/P2 slots = User Defined

3U, 6-Slot Signal Assignments (BKP3-CEN06-15.2.2)

J0 Signal Assignments

	Row I	Row H	Row G	Row F	Row E	Row D	Row C	Row B	Row A
1	Vs1	Vs1	Vs1	Vs1	No Pad	Vs2	Vs2	Vs2	Vs2
2	Vs1	Vs1	Vs1	Vs1	No Pad	Vs2	Vs2	Vs2	Vs2
3	Vs3	Vs3	Vs3	Vs3	No Pad	Vs3	Vs3	Vs3	Vs3
4	GND	SM2	SM3	GND	-12V_Aux	GND	SYSRESET*	NVMRO	GND
5	GND	GAP*	GA4*	GND	3.3V_Aux	GND	SM0	SM1	GND
6	GND	GA3*	GA2*	GND	+12V_Aux	GND	GA1*	GA0*	GND
7	TCK	GND	GND	TDO	TDI	GND	GND	TMS	TRST*
8	GND	REF_CLK-	REF_CLK+	GND	GND	AUX_CLK-	AUX_CLK+	GND	GND

J1/P1 Payload Signal Assignments

Plug-in Module P1		Row G	Row F	Row E Even	Row E Odd	Row D	Row C	Row B Even	Row B Odd	Row A
Bplane J1		Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a
1	Data Plane Port 1 / x4 / 2x2 / 4x1	GDiscrete1	GND	GND-J1	DP01-TD0-	DP01-TD0+	GND	GND-J1	DP01-RD0-	DP01-RD0+
2		GND	DP01-TD1-	DP01-TD1+	GND-J1	GND	DP01-RD1-	DP01-RD1+	GND-J1	GND
3		P1-VBAT	GND	GND-J1	DP01-TD2-	DP01-TD2+	GND	GND-J1	DP01-RD2-	DP01-RD2+
4		GND	DP01-TD3-	DP01-TD3+	GND-J1	GND	DP01-RD3-	DP01-RD3+	GND-J1	GND
5	Expan. Plane Port 1 / x8 / x4 / 2x2 / 4x1	SYS_CON*	GND	GND-J1	EP00-TD-	EP00-TD+	GND	GND-J1	EP00-RD-	EP00-RD+
6		GND	EP01-TD-	EP01-TD+	GND-J1	GND	EP01-RD-	EP01-RD+	GND-J1	GND
7		Reserved	GND	GND-J1	EP02-TD-	EP02-TD+	GND	GND-J1	EP02-RD-	EP02-RD+
8		GND	EP03-TD-	EP03-TD+	GND-J1	GND	EP03-RD-	EP03-RD+	GND-J1	GND
9	Expan. Plane Port 2 / x4 / 2x2 / 4x1	UD	GND	GND-J1	EP04-TD-	EP04-TD+	GND	GND-J1	EP04-RD-	EP04-RD+
10		GND	EP05-TD-	EP05-TD+	GND-J1	GND	EP05-RD-	EP05-RD+	GND-J1	GND
11		UD	GND	GND-J1	EP06-TD-	EP06-TD+	GND	GND-J1	EP06-RD-	EP06-RD+
12		GND	EP07-TD-	EP07-TD+	GND-J1	GND	EP07-RD-	EP07-RD+	GND-J1	GND
13	User Defined	UD	GND	GND-J1	UD	UD	GND	GND-J1	UD	UD
14		GND	UD	UD	GND-J1	GND	UD	UD	GND-J1	GND
15	Control Plane	Maskable Reset*	GND	GND-J1	CPutp02-TD-	CPutp02-TD+	GND	GND-J1	CPutp02-RD-	CPutp02-RD+
16		GND	CPutp01-TD-	CPutp01-TD+	GND-J1	GND	CPutp01-RD-	CPutp01-RD+	GND-J1	GND

J1/P1 Switch Signal Assignments

Plug-in Module P1		Row G	Row F	Row E Even	Row E Odd	Row D	Row C	Row B Even	Row B Odd	Row A
Bplane J1		Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a
1	Data Plane Port 1	GDiscrete1	GND	GND-J1	DP01-TD0-	DP01-TD0+	GND	GND-J1	DP01-RD0-	DP01-RD0+
2		GND	DP01-TD1-	DP01-TD1+	GND-J1	GND	DP01-RD1-	DP01-RD1+	GND-J1	GND
3		P1-VBAT	GND	GND-J1	DP01-TD2-	DP01-TD2+	GND	GND-J1	DP01-RD2-	DP01-RD2+
4		GND	DP01-TD3-	DP01-TD3+	GND-J1	GND	DP01-RD3-	DP01-RD3+	GND-J1	GND
5	Data Plane Port 2	SYS_CON*	GND	GND-J1	DP02-TD0-	DP02-TD0+	GND	GND-J1	DP02-RD0-	DP02-RD0+
6		GND	DP02-TD1-	DP02-TD1+	GND-J1	GND	DP02-RD1-	DP02-RD1+	GND-J1	GND
7		Reserved	GND	GND-J1	DP02-TD2-	DP02-TD2+	GND	GND-J1	DP02-RD2-	DP02-RD2+
8		GND	DP02-TD3-	DP02-TD3+	GND-J1	GND	DP02-RD3-	DP02-RD3+	GND-J1	GND
9	Data Plane Port 3	UD	GND	GND-J1	DP03-TD0-	DP03-TD0+	GND	GND-J1	DP03-RD0-	DP03-RD0+
10		GND	DP03-TD1-	DP03-TD1+	GND-J1	GND	DP03-RD1-	DP03-RD1+	GND-J1	GND
11		UD	GND	GND-J1	DP03-TD2-	DP03-TD2+	GND	GND-J1	DP03-RD2-	DP03-RD2+
12		GND	DP03-TD3-	DP03-TD3+	GND-J1	GND	DP03-RD3-	DP03-RD3+	GND-J1	GND
13	Data Plane Port 4	UD	GND	GND-J1	DP04-TD0-	DP04-TD0+	GND	GND-J1	DP04-RD0-	DP04-RD0+
14		GND	DP04-TD1-	DP04-TD1+	GND-J1	GND	DP04-RD1-	DP04-RD1+	GND-J1	GND
15		Maskable Reset*	GND	GND-J1	DP04-TD2-	DP04-TD2+	GND	GND-J1	DP04-RD2-	DP04-RD2+
16		GND	DP04-TD3-	DP04-TD3+	GND-J1	GND	DP04-RD3-	DP04-RD3+	GND-J1	GND

J2/P2 Switch Signal Assignments

Plug-in Module P2		Row G	Row F	Row E Even	Row E Odd	Row D	Row C	Row B Even	Row B Odd	Row A
Bplane J2		Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a
1	Data Plane Port 5	UD	GND	GND-J2	DP05-TD0-	DP05-TD0+	GND	GND-J2	DP05-RD0-	DP05-RD0+
2		GND	DP05-TD1-	DP05-TD1+	GND-J2	GND	DP05-RD1-	DP05-RD1+	GND-J2	GND
3		UD	GND	GND-J2	DP05-TD2-	DP05-TD2+	GND	GND-J2	DP05-RD2-	DP05-RD2+
4		GND	DP05-TD3-	DP05-TD3+	GND-J2	GND	DP05-RD3-	DP05-RD3+	GND-J2	GND
5	Data Plane Port 6	UD	GND	GND-J2	DS01-TD0-	DS01-TD0+	GND	GND-J2	DS01-RD0-	DS01-RD0+
6		GND	DS01-TD1-	DS01-TD1+	GND-J2	GND	DS01-RD1-	DS01-RD1+	GND-J2	GND
7		UD	GND	GND-J2	DS01-TD2-	DS01-TD2+	GND	GND-J2	DS01-RD2-	DS01-RD2+
8		GND	DS01-TD3-	DS01-TD3+	GND-J2	GND	DS01-RD3-	DS01-RD3+	GND-J2	GND
9	Control Plane Ports 1 - 6	UD	GND	GND-J2	CSutp01-TD-	CSutp01-TD+	GND	GND-J2	CSutp01-RD-	CSutp01-RD+
10		GND	CPutp06-TD-	CPutp06-TD+	GND-J2	GND	CPutp06-RD-	CPutp06-RD+	GND-J2	GND
11		UD	GND	GND-J2	CPutp04-TD-	CPutp04-TD+	GND	GND-J2	CPutp04-RD-	CPutp04-RD+
12		GND	CPutp03-TD-	CPutp03-TD+	GND-J2	GND	CPutp03-RD-	CPutp03-RD+	GND-J2	GND
13		UD	GND	GND-J2	CPutp02-TD-	CPutp02-TD+	GND	GND-J2	CPutp02-RD-	CPutp02-RD+
14		GND	CPutp01-TD-	CPutp01-TD+	GND-J2	GND	CPutp01-RD-	CPutp01-RD+	GND-J2	GND
15	UD	UD	GND	GND-J2	UD	UD	GND	GND-J2	UD	UD
16		GND	UD	UD	GND-J2	GND	UD	UD	GND-J2	GND

User Defined Pins for Thin Pipe - P2 & J2

3U, 9-Slot Signal Assignments

J0 Signal Assignments

	Row I	Row H	Row G	Row F	Row E	Row D	Row C	Row B	Row A
1	Vs1	Vs1	Vs1	Vs1	No Pad	Vs2	Vs2	Vs2	Vs2
2	Vs1	Vs1	Vs1	Vs1	No Pad	Vs2	Vs2	Vs2	Vs2
3	Vs3	Vs3	Vs3	Vs3	No Pad	Vs3	Vs3	Vs3	Vs3
4	GND	SM2	SM3	GND	-12V_Aux	GND	SYSRESET*	NVMRO	GND
5	GND	GAP*	GA4*	GND	3.3V_Aux	GND	SM0	SM1	GND
6	GND	GA3*	GA2*	GND	+12V_Aux	GND	GA1*	GA0*	GND
7	TCK	GND	GND	TDO	TDI	GND	GND	TMS	TRST*
8	GND	REF_CLK-	REF_CLK+	GND	GND	AUX_CLK-	AUX_CLK+	GND	GND

J1/P1 Signal Assignments for Slot 1

Plug-in module P1		Row G	Row F	Row E Even	Row E Odd	Row D	Row C	Row B Even	Row B Odd	Row A
Bplane J1		Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a
1	Data Plane Port 1 / X8 / x4 / 2x2 / 4x1	GDiscrete1	GND	GND-J1	DP01-TD0-	DP01-TD0+	GND	GND-J1	DP01-RD0-	DP01-RD0+
2		GND	DP01-TD1-	DP01-TD1+	GND-J1	GND	DP01-RD1-	DP01-RD1+	GND-J1	GND
3		P1-VBAT	GND	GND-J1	DP01-TD2-	DP01-TD2+	GND	GND-J1	DP01-RD2-	DP01-RD2+
4		GND	DP01-TD3-	DP01-TD3+	GND-J1	GND	DP01-RD3-	DP01-RD3+	GND-J1	GND
5	Data Plane Port 2 / x4 / 2x2 / 4x1	SYS_CON*	GND	GND-J1	DP02-TD0-	DP02-TD0+	GND	GND-J1	DP02-RD0-	DP02-RD0+
6		GND	DP02-TD1-	DP02-TD1+	GND-J1	GND	DP02-RD1-	DP02-RD1+	GND-J1	GND
7		Reserved	GND	GND-J1	DP02-TD2-	DP02-TD2+	GND	GND-J1	DP02-RD2-	DP02-RD2+
8		GND	DP02-TD3-	DP02-TD3+	GND-J1	GND	DP02-RD3-	DP02-RD3+	GND-J1	GND
9	User Defined	UD	GND	GND-J1	UD	UD	GND	GND-J1	UD	UD
10		GND	UD	UD	GND-J1	GND	UD	UD	GND-J1	GND
11		UD	GND	GND-J1	UD	UD	GND	GND-J1	UD	UD
12		GND	UD	UD	GND-J1	GND	UD	UD	GND-J1	GND
13		UD	GND	GND-J1	UD	UD	GND	GND-J1	UD	UD
14		GND	UD	UD	GND-J1	GND	UD	UD	GND-J1	GND
15	Control Plane	Maskable Reset*	GND	GND-J1	CPutp02-TD-	CPutp02-TD+	GND	GND-J1	CPutp02-RD-	CPutp02-RD+
16		GND	CPutp01-TD-	CPutp01-TD+	GND-J1	GND	CPutp01-RD-	CPutp01-RD+	GND-J1	GND

J1/P1 Signal Assignments for Slots 2, 3 & 5

Plug-in module P1		Row G	Row F	Row E Even	Row E Odd	Row D	Row C	Row B Even	Row B Odd	Row A
Bplane J1		Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a
1	Data Plane Port 1 / 1x4 / 2x2 / 4x1	GDiscrete1	GND	GND-J1	DP01-TD0-	DP01-TD0+	GND	GND-J1	DP01-RD0-	DP01-RD0+
2		GND	DP01-TD1-	DP01-TD1+	GND-J1	GND	DP01-RD1-	DP01-RD1+	GND-J1	GND
3		P1-VBAT	GND	GND-J1	DP01-TD2-	DP01-TD2+	GND	GND-J1	DP01-RD2-	DP01-RD2+
4		GND	DP01-TD3-	DP01-TD3+	GND-J1	GND	DP01-RD3-	DP01-RD3+	GND-J1	GND
5	User Defined	SYS_CON*	GND	GND-J1	UD	UD	GND	GND-J1	UD	UD
6		GND	UD	UD	GND-J1	GND	UD	UD	GND-J1	GND
7		Reserved	GND	GND-J1	UD	UD	GND	GND-J1	UD	UD
8		GND	UD	UD	GND-J1	GND	UD	UD	GND-J1	GND
9		UD	GND	GND-J1	UD	UD	GND	GND-J1	UD	UD
10		GND	UD	UD	GND-J1	GND	UD	UD	GND-J1	GND
11		UD	GND	GND-J1	UD	UD	GND	GND-J1	UD	UD
12		GND	UD	UD	GND-J1	GND	UD	UD	GND-J1	GND
13		UD	GND	GND-J1	UD	UD	GND	GND-J1	UD	UD
14		GND	UD	UD	GND-J1	GND	UD	UD	GND-J1	GND
15	Control Plane	Maskable Reset*	GND	GND-J1	CPutp02-TD-	CPutp02-TD+	GND	GND-J1	CPutp02-RD-	CPutp02-RD+
16		GND	CPutp01-TD-	CPutp01-TD+	GND-J1	GND	CPutp01-RD-	CPutp01-RD+	GND-J1	GND

J1/P1 Signal Assignments for Slot 4

Plug-in Module P1		Row G	Row F	Row E Even	Row E Odd	Row D	Row C	Row B Even	Row B Odd	Row A
Bplane J1		Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a
1	Data Plane Port 1	GDiscrete1	GND	GND-J1	DP01-TD0-	DP01-TD0+	GND	GND-J1	DP01-RD0-	DP01-RD0+
2		GND	DP01-TD1-	DP01-TD1+	GND-J1	GND	DP01-RD1-	DP01-RD1+	GND-J1	GND
3		P1-VBAT	GND	GND-J1	DP01-TD2-	DP01-TD2+	GND	GND-J1	DP01-RD2-	DP01-RD2+
4		GND	DP01-TD3-	DP01-TD3+	GND-J1	GND	DP01-RD3-	DP01-RD3+	GND-J1	GND
5	Data Plane Port 2	SYS_CON*	GND	GND-J1	DP02-TD0-	DP02-TD0+	GND	GND-J1	DP02-RD0-	DP02-RD0+
6		GND	DP02-TD1-	DP02-TD1+	GND-J1	GND	DP02-RD1-	DP02-RD1+	GND-J1	GND
7		Reserved	GND	GND-J1	DP02-TD2-	DP02-TD2+	GND	GND-J1	DP02-RD2-	DP02-RD2+
8		GND	DP02-TD3-	DP02-TD3+	GND-J1	GND	DP02-RD3-	DP02-RD3+	GND-J1	GND
9	Data Plane Port 3	UD	GND	GND-J1	DP03-TD0-	DP03-TD0+	GND	GND-J1	DP03-RD0-	DP03-RD0+
10		GND	DP03-TD1-	DP03-TD1+	GND-J1	GND	DP03-RD1-	DP03-RD1+	GND-J1	GND
11		UD	GND	GND-J1	DP03-TD2-	DP03-TD2+	GND	GND-J1	DP03-RD2-	DP03-RD2+
12		GND	DP03-TD3-	DP03-TD3+	GND-J1	GND	DP03-RD3-	DP03-RD3+	GND-J1	GND
13	Data Plane Port 4	UD	GND	GND-J1	DP04-TD0-	DP04-TD0+	GND	GND-J1	DP04-RD0-	DP04-RD0+
14		GND	DP04-TD1-	DP04-TD1+	GND-J1	GND	DP04-RD1-	DP04-RD1+	GND-J1	GND
15		Maskable Reset*	GND	GND-J1	DP04-TD2-	DP04-TD2+	GND	GND-J1	DP04-RD2-	DP04-RD2+
16		GND	DP04-TD3-	DP04-TD3+	GND-J1	GND	DP04-RD3-	DP04-RD3+	GND-J1	GND

J1/P1 Signal Assignments for Slots 6-9

Plug-in Module P1		Row G	Row F	Row E Even	Row E Odd	Row D	Row C	Row B Even	Row B Odd	Row A
Bplane J1		Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a
1	Data Plane Port 1 / x4 / 2x2 / 4x1	GDiscrete1	GND	GND-J1	DP01-TD0-	DP01-TD0+	GND	GND-J1	DP01-RD0-	DP01-RD0+
2		GND	DP01-TD1-	DP01-TD1+	GND-J1	GND	DP01-RD1-	DP01-RD1+	GND-J1	GND
3		P1-VBAT	GND	GND-J1	DP01-TD2-	DP01-TD2+	GND	GND-J1	DP01-RD2-	DP01-RD2+
4		GND	DP01-TD3-	DP01-TD3+	GND-J1	GND	DP01-RD3-	DP01-RD3+	GND-J1	GND
5	Expan. Plane Port 1 / x8 / x4 / 2x2 / 4x1	SYS_CON*	GND	GND-J1	EP00-TD-	EP00-TD+	GND	GND-J1	EP00-RD-	EP00-RD+
6		GND	EP01-TD-	EP01-TD+	GND-J1	GND	EP01-RD-	EP01-RD+	GND-J1	GND
7		Reserved	GND	GND-J1	EP02-TD-	EP02-TD+	GND	GND-J1	EP02-RD-	EP02-RD+
8		GND	EP03-TD-	EP03-TD+	GND-J1	GND	EP03-RD-	EP03-RD+	GND-J1	GND
9	Expan. Plane Port 2 / x4 / 2x2 / 4x1	UD	GND	GND-J1	EP04-TD-	EP04-TD+	GND	GND-J1	EP04-RD-	EP04-RD+
10		GND	EP05-TD-	EP05-TD+	GND-J1	GND	EP05-RD-	EP05-RD+	GND-J1	GND
11		UD	GND	GND-J1	EP06-TD-	EP06-TD+	GND	GND-J1	EP06-RD-	EP06-RD+
12		GND	EP07-TD-	EP07-TD+	GND-J1	GND	EP07-RD-	EP07-RD+	GND-J1	GND
13	User Defined	UD	GND	GND-J1	UD	UD	GND	GND-J1	UD	UD
14		GND	UD	UD	GND-J1	GND	UD	UD	GND-J1	GND
15	Control Plane	Maskable Reset*	GND	GND-J1	CPutp02-TD-	CPutp02-TD+	GND	GND-J1	CPutp02-RD-	CPutp02-RD+
16		GND	CPutp01-TD-	CPutp01-TD+	GND-J1	GND	CPutp01-RD-	CPutp01-RD+	GND-J1	GND

J2/P2 Signal Assignments for Slot 4

Plug-in Module P2		Row G	Row F	Row E Even	Row E Odd	Row D	Row C	Row B Even	Row B Odd	Row A
Bplane J2		Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a
1	Data Plane Port 5	UD	GND	GND-J2	DP05-TD0-	DP05-TD0+	GND	GND-J2	DP05-RD0-	DP05-RD0+
2		GND	DP05-TD1-	DP05-TD1+	GND-J2	GND	DP05-RD1-	DP05-RD1+	GND-J2	GND
3		UD	GND	GND-J2	DP05-TD2-	DP05-TD2+	GND	GND-J2	DP05-RD2-	DP05-RD2+
4		GND	DP05-TD3-	DP05-TD3+	GND-J2	GND	DP05-RD3-	DP05-RD3+	GND-J2	GND
5	Data Plane Port 6	UD	GND	GND-J2	DS01-TD0-	DS01-TD0+	GND	GND-J2	DS01-RD0-	DS01-RD0+
6		GND	DS01-TD1-	DS01-TD1+	GND-J2	GND	DS01-RD1-	DS01-RD1+	GND-J2	GND
7		UD	GND	GND-J2	DS01-TD2-	DS01-TD2+	GND	GND-J2	DS01-RD2-	DS01-RD2+
8		GND	DS01-TD3-	DS01-TD3+	GND-J2	GND	DS01-RD3-	DS01-RD3+	GND-J2	GND
9	Control Plane Ports 1 - 8	UD	GND	GND-J2	CSutp01-TD-	CSutp01-TD+	GND	GND-J2	CSutp01-RD-	CSutp01-RD+
10		GND	CPutp05-TD-	CPutp05-TD+	GND-J2	GND	CPutp05-RD-	CPutp05-RD+	GND-J2	GND
11		UD	GND	GND-J2	CPutp04-TD-	CPutp04-TD+	GND	GND-J2	CPutp04-RD-	CPutp04-RD+
12		GND	CPutp03-TD-	CPutp03-TD+	GND-J2	GND	CPutp03-RD-	CPutp03-RD+	GND-J2	GND
13		UD	GND	GND-J2	CPutp02-TD-	CPutp02-TD+	GND	GND-J2	CPutp02-RD-	CPutp02-RD+
14		GND	CPutp01-TD-	CPutp01-TD+	GND-J2	GND	CPutp01-RD-	CPutp01-RD+	GND-J2	GND
15		UD	GND	GND-J2	Cputp07-TD-	Cputp07-TD+	GND	GND-J2	Cputp07-RD-	Cputp07-RD+
16		GND	CPutp06-TD-	CPutp06-TD+	GND-J2	GND	CPutp06-RD-	CPutp06-RD+	GND-J2	GND

*J2 slots 1-3 and 5-9 = User Defined

VITA Based Backplanes

6U, 5-Slot Signal Assignments

J0 Signal Assignments

	Row I	Row H	Row G	Row F	Row E	Row D	Row C	Row B	Row A
1	Vs1	Vs1	Vs1	Vs1	No Pad	Vs2	Vs2	Vs2	Vs2
2	Vs1	Vs1	Vs1	Vs1	No Pad	Vs2	Vs2	Vs2	Vs2
3	Vs3	Vs3	Vs3	Vs3	No Pad	Vs3	Vs3	Vs3	Vs3
4	GND	SM2	SM3	GND	-12V_Aux	GND	SYSRESET*	NVMRO	GND
5	GND	GAP*	GA4*	GND	3.3V_Aux	GND	SM0	SM1	GND
6	GND	GA3*	GA2*	GND	+12V_Aux	GND	GA1*	GA0*	GND
7	TCK	GND	GND	TDO	TDI	GND	GND	TMS	TRST*
8	GND	REF_CLK-	REF_CLK+	GND	GND	AUX_CLK-	AUX_CLK+	GND	GND

J2-J6 Signal Assignments = User Defined

J1/P1 Signal Assignments

Plug-in Module P1		Row G	Row F	Row E Even	Row E Odd	Row D	Row C	Row B Even	Row B Odd	Row A
Bplane J1		Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a
1	Data Plane Port 1	GDiscrete1	GND	GND-J1	DP01-T0-	DP01-T0+	GND	GND-J1	DP01-R0-	DP01-R0+
2		GND	DP01-T1-	DP01-T1+	GND-J1	GND	DP01-R1-	DP01-R1+	GND-J1	GND
3		P1-VBAT	GND	GND-J1	DP01-T2-	DP01-T2+	GND	GND-J1	DP01-R2-	DP01-R2+
4		GND	DP01-T3-	DP01-T3+	GND-J1	GND	DP01-R3-	DP01-R3+	GND-J1	GND
5	Data Plane Port 2	SYS_CON*	GND	GND-J1	DP02-T0-	DP02-T0+	GND	GND-J1	DP02-R0-	DP02-R0+
6		GND	DP02-T1-	DP02-T1+	GND-J1	GND	DP02-R1-	DP02-R1+	GND-J1	GND
7		Reserved	GND	GND-J1	DP02-T2-	DP02-T2+	GND	GND-J1	DP02-R2-	DP02-R2+
8		GND	DP02-T3-	DP02-T3+	GND-J1	GND	DP02-R3-	DP02-R3+	GND-J1	GND
9	Data Plane Port 3	UD	GND	GND-J1	DP03-T0-	DP03-T0+	GND	GND-J1	DP03-R0-	DP03-R0+
10		GND	DP03-T1-	DP03-T1+	GND-J1	GND	DP03-R1-	DP03-R1+	GND-J1	GND
11		UD	GND	GND-J1	DP03-T2-	DP03-T2+	GND	GND-J1	DP03-R2-	DP03-R2+
12		GND	DP03-T3-	DP03-T3+	GND-J1	GND	DP03-R3-	DP03-R3+	GND-J1	GND
13	Data Plane Port 4	UD	GND	GND-J1	DP04-T0-	DP04-T0+	GND	GND-J1	DP04-R0-	DP04-R0+
14		GND	DP04-T1-	DP04-T1+	GND-J1	GND	DP04-R1-	DP04-R1+	GND-J1	GND
15		Maskable Reset*	GND	GND-J1	DP04-T2-	DP04-T2+	GND	GND-J1	DP04-R2-	DP04-R2+
16		GND	DP04-T3-	DP04-T3+	GND-J1	GND	DP04-R3-	DP04-R3+	GND-J1	GND

6U, 5-Slot Payload Signal Assignments (BKP6-CEN05-11.2.5)

J0 Signal Assignments

	Row I	Row H	Row G	Row F	Row E	Row D	Row C	Row B	Row A
1	Vs1	Vs1	Vs1	Vs1	No Pad	Vs2	Vs2	Vs2	Vs2
2	Vs1	Vs1	Vs1	Vs1	No Pad	Vs2	Vs2	Vs2	Vs2
3	Vs3	Vs3	Vs3	Vs3	No Pad	Vs3	Vs3	Vs3	Vs3
4	GND	SM2	SM3	GND	-12V_Aux	GND	SYSRESET*	NVMRO	GND
5	GND	GAP*	GA4*	GND	3.3V_Aux	GND	SM0	SM1	GND
6	GND	GA3*	GA2*	GND	+12V_Aux	GND	GA1*	GA0*	GND
7	TCK	GND	GND	TDO	TDI	GND	GND	TMS	TRST*
8	GND	REF_CLK-	REF_CLK+	GND	GND	AUX_CLK-	AUX_CLK+	GND	GND

J1/P1 Signal Assignments

Plug-in Module P1		Row G	Row F	Row E Even	Row E Odd	Row D	Row C	Row B Even	Row B Odd	Row A
Bplane J1		Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a
1	Data Plane Port 1	GDiscrete1	GND	GND-J1	DP01-T0-	DP01-T0+	GND	GND-J1	DP01-R0-	DP01-R0+
2		GND	DP01-T1-	DP01-T1+	GND-J1	GND	DP01-R1-	DP01-R1+	GND-J1	GND
3		P1-VBAT	GND	GND-J1	DP01-T2-	DP01-T2+	GND	GND-J1	DP01-R2-	DP01-R2+
4		GND	DP01-T3-	DP01-T3+	GND-J1	GND	DP01-R3-	DP01-R3+	GND-J1	GND
5	Data Plane Port 2	SYS_CON*	GND	GND-J1	DP02-T0-	DP02-T0+	GND	GND-J1	DP02-R0-	DP02-R0+
6		GND	DP02-T1-	DP02-T1+	GND-J1	GND	DP02-R1-	DP02-R1+	GND-J1	GND
7		Reserved	GND	GND-J1	DP02-T2-	DP02-T2+	GND	GND-J1	DP02-R2-	DP02-R2+
8		GND	DP02-T3-	DP02-T3+	GND-J1	GND	DP02-R3-	DP02-R3+	GND-J1	GND
9	Data Plane Port 3	UD	GND	GND-J1	DP03-T0-	DP03-T0+	GND	GND-J1	DP03-R0-	DP03-R0+
10		GND	DP03-T1-	DP03-T1+	GND-J1	GND	DP03-R1-	DP03-R1+	GND-J1	GND
11		UD	GND	GND-J1	DP03-T2-	DP03-T2+	GND	GND-J1	DP03-R2-	DP03-R2+
12		GND	DP03-T3-	DP03-T3+	GND-J1	GND	DP03-R3-	DP03-R3+	GND-J1	GND
13	Data Plane Port 4	UD	GND	GND-J1	DP04-T0-	DP04-T0+	GND	GND-J1	DP04-R0-	DP04-R0+
14		GND	DP04-T1-	DP04-T1+	GND-J1	GND	DP04-R1-	DP04-R1+	GND-J1	GND
15		Maskable Reset*	GND	GND-J1	DP04-T2-	DP04-T2+	GND	GND-J1	DP04-R2-	DP04-R2+
16		GND	DP04-T3-	DP04-T3+	GND-J1	GND	DP04-R3-	DP04-R3+	GND-J1	GND

J2/P2 Signal Assignments

Plug-In Module P2				Row G	Row F	Row E Even	Row E Odd	Row D	Row C	Row B Even	Row B Odd	Row A
Backplane J2				Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a
1	X16 using [15:0]	x8 using [7:0]	x4 using [3:0]	UD	GND	GND-J2	EP00-T-	EP00-T+	GND	GND-J2	EP00-R-	EP00-R+
2				GND	EP01-T-	EP01-T+	GND-J2	GND	EP01-R-	EP01-R+	GND-J2	GND
3				UD	GND	GND-J2	EP02-T-	EP02-T+	GND	GND-J2	EP02-R-	EP02-R+
4				GND	EP03-T-	EP03-T+	GND-J2	GND	EP03-R-	EP03-R+	GND-J2	GND
5			x4 using [7:4]	UD	GND	GND-J2	EP04-T-	EP04-T+	GND	GND-J2	EP04-R-	EP04-R+
6				GND	EP05-T-	EP05-T+	GND-J2	GND	EP05-R-	EP05-R+	GND-J2	GND
7				UD	GND	GND-J2	EP06-T-	EP06-T+	GND	GND-J2	EP06-R-	EP06-R+
8				GND	EP07-T-	EP07-T+	GND-J2	GND	EP07-R-	EP07-R+	GND-J2	GND
9		x8 using[15:8]	x4 using [11:8]	UD	GND	GND-J2	EP08-T-	EP08-T+	GND	GND-J2	EP08-R-	EP08-R+
10				GND	EP09-T-	EP09-T+	GND-J2	GND	EP09-R-	EP09-R+	GND-J2	GND
11				UD	GND	GND-J2	EP10-T-	EP10-T+	GND	GND-J2	EP10-R-	EP10-R+
12				GND	EP11-T-	EP11-T+	GND-J2	GND	EP11-R-	EP11-R+	GND-J2	GND
13			x4 using[15:12]	UD	GND	GND-J2	EP12-T-	EP12-T+	GND	GND-J2	EP12-R-	EP12-R+
14				GND	EP13-T-	EP13-T+	GND-J2	GND	EP13-R-	EP13-R+	GND-J2	GND
15				UD	GND	GND-J2	EP14-T-	EP14-T+	GND	GND-J2	EP14-R-	EP14-R+
16				GND	EP15-T-	EP15-T+	GND-J2	GND	EP15-R-	EP15-R+	GND-J2	GND

J3, J5-J6 Signal Assignments = User Defined

J4/P4 Signal Assignments

Plug-in Mod P4		Row G	Row F	Row E Even	Row E Odd	Row D	Row C	Row B Even	Row B Odd	Row A
Bplane J4		Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a
1	User Defined	UD	GND	GND-J4	UD	UD	GND	GND-J4	UD	UD
2		GND	UD	UD	GND-J4	GND	UD	UD	GND-J4	GND
3		UD	GND	GND-J4	UD	UD	GND	GND-J4	UD	UD
4		GND	UD	UD	GND-J4	GND	UD	UD	GND-J4	GND
5		UD	GND	GND-J4	UD	UD	GND	GND-J4	UD	UD
6		GND	UD	UD	GND-J4	GND	UD	UD	GND-J4	GND
7		UD	GND	GND-J4	UD	UD	GND	GND-J4	UD	UD
8		GND	UD	UD	GND-J4	GND	UD	UD	GND-J4	GND
9		UD	GND	GND-J4	UD	UD	GND	GND-J4	UD	UD
10		GND	UD	UD	GND-J4	GND	UD	UD	GND-J4	GND
11	2 UTP	UD	GND	GND-J4	CPutp02-T-	CPutp02-T+	GND	GND-J4	CPutp02-R-	CPutp02-R+
12		GND	CPutp01-T-	CPutp01-T+	GND-J4	GND	CPutp01-R-	CPutp01-R+	GND-J4	GND
13	Control Plane 2 TPs	UD	GND	GND-J4	CPtp02-DB-	CPtp02-DB+	GND	GND-J4	CPtp02-DA-	CPtp02-DA+
14		GND	CPtp02-DD-	CPtp02-DD+	GND-J4	GND	CPtp02-DC-	CPtp02-DC+	GND-J4	GND
15		UD	GND	GND-J4	CPtp01-DB-	CPtp01-DB+	GND	GND-J4	CPtp01-DA-	CPtp01-DA+
16		GND	CPtp01-DD-	CPtp01-DD+	GND-J4	GND	CPtp01-DC-	CPtp01-DC+	GND-J4	GND

6U, 5-Slot Switch Signal Assignments (BKP6-CEN05-11.2.5)

J1/P1 Signal Assignments

Plug-in Module P1		Row G	Row F	Row E Even	Row E Odd	Row D	Row C	Row B Even	Row B Odd	Row A
Bplane J1		Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a
1	CPlane (switch) UTPs Ports 1 - 4	GDiscrete1	GND	GND-J1	CSutp01-T-	CSutp01-T+	GND	GND-J1	CSutp01-R-	CSutp01-R+
2		GND	CSutp02-T-	CSutp02-T+	GND-J1	GND	CSutp02-R-	CSutp02-R+	GND-J1	GND
3		P1-VBAT	GND	GND-J1	CSutp03-T-	CSutp03-T+	GND	GND-J1	CSutp03-R-	CSutp03-R+
4		GND	CSutp04-T-	CSutp04-T+	GND-J1	GND	CSutp04-R-	CSutp04-R+	GND-J1	GND
5	Control Plane Payload UTPs Ports 1 - 12	SYS_CON*	GND	GND-J1	CPutp01-T-	CPutp01-T+	GND	GND-J1	CPutp01-R-	CPutp01-R+
6		GND	CPutp02-T-	CPutp02-T+	GND-J1	GND	CPutp02-R-	CPutp02-R+	GND-J1	GND
7		Reserved	GND	GND-J1	CPutp03-T-	CPutp03-T+	GND	GND-J1	CPutp03-R-	CPutp03-R+
8		GND	CPutp04-T-	CPutp04-T+	GND-J1	GND	CPutp04-R-	CPutp04-R+	GND-J1	GND
9		UD	GND	GND-J1	CPutp05-T-	CPutp05-T+	GND	GND-J1	CPutp05-R-	CPutp05-R+
10		GND	CPutp06-T-	CPutp06-T+	GND-J1	GND	CPutp06-R-	CPutp06-R+	GND-J1	GND
11		UD	GND	GND-J1	CPutp07-T-	CPutp07-T+	GND	GND-J1	CPutp07-R-	CPutp07-R+
12		GND	CPutp08-T-	CPutp08-T+	GND-J1	GND	CPutp08-R-	CPutp08-R+	GND-J1	GND
13		UD	GND	GND-J1	CPutp09-T-	CPutp09-T+	GND	GND-J1	CPutp09-R-	CPutp09-R+
14		GND	CPutp10-T-	CPutp10-T+	GND-J1	GND	CPutp10-R-	CPutp10-R+	GND-J1	GND
15		Maskable Reset*	GND	GND-J1	CPutp11-T-	CPutp11-T+	GND	GND-J1	CPutp11-R-	CPutp11-R+
16		GND	CPutp12-T-	CPutp12-T+	GND-J1	GND	CPutp12-R-	CPutp12-R+	GND-J1	GND

J2/P2 Signal Assignments

Plug-in Module P2		Row G	Row F	Row E Even	Row E Odd	Row D	Row C	Row B Even	Row B Odd	Row A
Bplane J2		Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a
1	Data Plane FP Port 16	UD	GND	GND-J2	DP16-T0-	DP16-T0+	GND	GND-J2	DP16-R0-	DP16-R0+
2		GND	DP16-T1-	DP16-T1+	GND-J2	GND	DP16-R1-	DP16-R1+	GND-J2	GND
3		UD	GND	GND-J2	DP16-T2-	DP16-T2+	GND	GND-J2	DP16-R2-	DP16-R2+
4		GND	DP16-T3-	DP16-T3+	GND-J2	GND	DP16-R3-	DP16-R3+	GND-J2	GND
5	Data Plane FP Port 15	UD	GND	GND-J2	DP15-T0-	DP15-T0+	GND	GND-J2	DP15-R0-	DP15-R0+
6		GND	DP15-T1-	DP15-T1+	GND-J2	GND	DP15-R1-	DP15-R1+	GND-J2	GND
7		UD	GND	GND-J2	DP15-T2-	DP15-T2+	GND	GND-J2	DP15-R2-	DP15-R2+
8		GND	DP15-T3-	DP15-T3+	GND-J2	GND	DP15-R3-	DP15-R3+	GND-J2	GND
9	Data Plane FP Port 14	UD	GND	GND-J2	DP14-T0-	DP14-T0+	GND	GND-J2	DP14-R0-	DP14-R0+
10		GND	DP14-T1-	DP14-T1+	GND-J2	GND	DP14-R1-	DP14-R1+	GND-J2	GND
11		UD	GND	GND-J2	DP14-T2-	DP14-T2+	GND	GND-J2	DP14-R2-	DP14-R2+
12		GND	DP14-T3-	DP14-T3+	GND-J2	GND	DP14-R3-	DP14-R3+	GND-J2	GND
13	Data Plane FP Port 13	UD	GND	GND-J2	DP13-T0-	DP13-T0+	GND	GND-J2	DP13-R0-	DP13-R0+
14		GND	DP13-T1-	DP13-T1+	GND-J2	GND	DP13-R1-	DP13-R1+	GND-J2	GND
15		UD	GND	GND-J2	DP13-T2-	DP13-T2+	GND	GND-J2	DP13-R2-	DP13-R2+
16		GND	DP13-T3-	DP13-T3+	GND-J2	GND	DP13-R3-	DP13-R3+	GND-J2	GND

J3/P3-J4/P4 Signal Assignments

Plug-in Module P3		Row G	Row F	Row E Even	Row E Odd	Row D	Row C	Row B Even	Row B Odd	Row A
Bplane J3		Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a
1	Data Plane Payload FP Port 12	UD	GND	GND-J3	DP12-T0-	DP12-T0+	GND	GND-J3	DP12-R0-	DP12-R0+
2		GND	DP12-T1-	DP12-T1+	GND-J3	GND	DP12-R1-	DP12-R1+	GND-J3	GND
3		UD	GND	GND-J3	DP12-T2-	DP12-T2+	GND	GND-J3	DP12-R2-	DP12-R2+
4		GND	DP12-T3-	DP12-T3+	GND-J3	GND	DP12-R3-	DP12-R3+	GND-J3	GND
5	Data Plane Payload FP Port 11	UD	GND	GND-J3	DP11-T0-	DP11-T0+	GND	GND-J3	DP11-R0-	DP11-R0+
6		GND	DP11-T1-	DP11-T1+	GND-J3	GND	DP11-R1-	DP11-R1+	GND-J3	GND
7		UD	GND	GND-J3	DP11-T2-	DP11-T2+	GND	GND-J3	DP11-R2-	DP11-R2+
8		GND	DP11-T3-	DP11-T3+	GND-J3	GND	DP11-R3-	DP11-R3+	GND-J3	GND
9	Data Plane Payload FP Port 10	UD	GND	GND-J3	DP10-T0-	DP10-T0+	GND	GND-J3	DP10-R0-	DP10-R0+
10		GND	DP10-T1-	DP10-T1+	GND-J3	GND	DP10-R1-	DP10-R1+	GND-J3	GND
11		UD	GND	GND-J3	DP10-T2-	DP10-T2+	GND	GND-J3	DP10-R2-	DP10-R2+
12		GND	DP10-T3-	DP10-T3+	GND-J3	GND	DP10-R3-	DP10-R3+	GND-J3	GND
13	Data Plane Payload FP Port 9	UD	GND	GND-J3	DP09-T0-	DP09-T0+	GND	GND-J3	DP09-R0-	DP09-R0+
14		GND	DP09-T1-	DP09-T1+	GND-J3	GND	DP09-R1-	DP09-R1+	GND-J3	GND
15		UD	GND	GND-J3	DP09-T2-	DP09-T2+	GND	GND-J3	DP09-R2-	DP09-R2+
16		GND	DP09-T3-	DP09-T3+	GND-J3	GND	DP09-R3-	DP09-R3+	GND-J3	GND

J5/P5-J6/P6 Signal Assignments

Plug-in Module P4		Row G	Row F	Row E		Row D	Row C	Row B		Row A
Bplane J4		Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a
1	Data Plane Payload FP Port 8	UD	GND	GND-J4	DP08-T0-	DP08-T0+	GND	GND-J4	DP08-R0-	DP08-R0+
2		GND	DP08-T1-	DP08-T1+	GND-J4	GND	DP08-R1-	DP08-R1+	GND-J4	GND
3		UD	GND	GND-J4	DP08-T2-	DP08-T2+	GND	GND-J4	DP08-R2-	DP08-R2+
4		GND	DP08-T3-	DP08-T3+	GND-J4	GND	DP08-R3-	DP08-R3+	GND-J4	GND
5	Data Plane Payload FP Port 7	UD	GND	GND-J4	DP07-T0-	DP07-T0+	GND	GND-J4	DP07-R0-	DP07-R0+
6		GND	DP07-T1-	DP07-T1+	GND-J4	GND	DP07-R1-	DP07-R1+	GND-J4	GND
7		UD	GND	GND-J4	DP07-T2-	DP07-T2+	GND	GND-J4	DP07-R2-	DP07-R2+
8		GND	DP07-T3-	DP07-T3+	GND-J4	GND	DP07-R3-	DP07-R3+	GND-J4	GND
9	Data Plane Payload FP Port 6	UD	GND	GND-J4	DP06-T0-	DP06-T0+	GND	GND-J4	DP06-R0-	DP06-R0+
10		GND	DP06-T1-	DP06-T1+	GND-J4	GND	DP06-R1-	DP06-R1+	GND-J4	GND
11		UD	GND	GND-J4	DP06-T2-	DP06-T2+	GND	GND-J4	DP06-R2-	DP06-R2+
12		GND	DP06-T3-	DP06-T3+	GND-J4	GND	DP06-R3-	DP06-R3+	GND-J4	GND
13	Data Plane Payload FP Port 5	UD	GND	GND-J4	DP05-T0-	DP05-T0+	GND	GND-J4	DP05-R0-	DP05-R0+
14		GND	DP05-T1-	DP05-T1+	GND-J4	GND	DP05-R1-	DP05-R1+	GND-J4	GND
15		UD	GND	GND-J4	DP05-T2-	DP05-T2+	GND	GND-J4	DP05-R2-	DP05-R2+
16		GND	DP05-T3-	DP05-T3+	GND-J4	GND	DP05-R3-	DP05-R3+	GND-J4	GND

6U, 6-Slot Signal Assignments (BKP6-DIS06-11.2.10)

J0 Signal Assignments

	Row I	Row H	Row G	Row F	Row E	Row D	Row C	Row B	Row A
1	Vs1	Vs1	Vs1	Vs1	No Pad	Vs2	Vs2	Vs2	Vs2
2	Vs1	Vs1	Vs1	Vs1	No Pad	Vs2	Vs2	Vs2	Vs2
3	Vs3	Vs3	Vs3	Vs3	No Pad	Vs3	Vs3	Vs3	Vs3
4	GND	SM2	SM3	GND	-12V_Aux	GND	SYSRESET*	NVMRO	GND
5	GND	GAP*	GA4*	GND	3.3V_Aux	GND	SM0	SM1	GND
6	GND	GA3*	GA2*	GND	+12V_Aux	GND	GA1*	GA0*	GND
7	TCK	GND	GND	TDO	TDI	GND	GND	TMS	TRST*
8	GND	REF_CLK-	REF_CLK+	GND	GND	AUX_CLK-	AUX_CLK+	GND	GND

J1/P1 Signal Assignments

Plug-in Module P1		Row G	Row F	Row E Even	Row E Odd	Row D	Row C	Row B Even	Row B Odd	Row A
Bplane J1		Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a
1	Data Plane Port 1	GDiscrete1	GND	GND-J1	DP01-T0-	DP01-T0+	GND	GND-J1	DP01-R0-	DP01-R0+
2		GND	DP01-T1-	DP01-T1+	GND-J1	GND	DP01-R1-	DP01-R1+	GND-J1	GND
3		P1-VBAT	GND	GND-J1	DP01-T2-	DP01-T2+	GND	GND-J1	DP01-R2-	DP01-R2+
4		GND	DP01-T3-	DP01-T3+	GND-J1	GND	DP01-R3-	DP01-R3+	GND-J1	GND
5	Data Plane Port 2	SYS_CON*	GND	GND-J1	DP02-T0-	DP02-T0+	GND	GND-J1	DP02-R0-	DP02-R0+
6		GND	DP02-T1-	DP02-T1+	GND-J1	GND	DP02-R1-	DP02-R1+	GND-J1	GND
7		Reserved	GND	GND-J1	DP02-T2-	DP02-T2+	GND	GND-J1	DP02-R2-	DP02-R2+
8		GND	DP02-T3-	DP02-T3+	GND-J1	GND	DP02-R3-	DP02-R3+	GND-J1	GND
9	Data Plane Port 3	UD	GND	GND-J1	DP03-T0-	DP03-T0+	GND	GND-J1	DP03-R0-	DP03-R0+
10		GND	DP03-T1-	DP03-T1+	GND-J1	GND	DP03-R1-	DP03-R1+	GND-J1	GND
11		UD	GND	GND-J1	DP03-T2-	DP03-T2+	GND	GND-J1	DP03-R2-	DP03-R2+
12		GND	DP03-T3-	DP03-T3+	GND-J1	GND	DP03-R3-	DP03-R3+	GND-J1	GND
13	Data Plane Port 4	UD	GND	GND-J1	DP04-T0-	DP04-T0+	GND	GND-J1	DP04-R0-	DP04-R0+
14		GND	DP04-T1-	DP04-T1+	GND-J1	GND	DP04-R1-	DP04-R1+	GND-J1	GND
15		Maskable Reset*	GND	GND-J1	DP04-T2-	DP04-T2+	GND	GND-J1	DP04-R2-	DP04-R2+
16		GND	DP04-T3-	DP04-T3+	GND-J1	GND	DP04-R3-	DP04-R3+	GND-J1	GND

J1/P1 Signal Assignments for Switch Slot 6

Plug-In Module P1		Row G	Row F	Row E Even	Row E Odd	Row D	Row C	Row B Even	Row B Odd	Row A
Bplane J1		Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a
1	Control Plane Port 1	GDiscrete1	GND	GND-J1	CP01-T0-	CP01-T0+	GND	GND-J1	CP01-R0-	CP01-R0+
2		GND	CP01-T1-	CP01-T1+	GND-J1	GND	CP01-R1-	CP01-R1+	GND-J1	GND
3		P1-VBAT	GND	GND-J1	CP01-T2-	CP01-T2+	GND	GND-J1	CP01-R2-	CP01-R2+
4		GND	CP01-T3-	CP01-T3+	GND-J1	GND	CP01-R3-	CP01-R3+	GND-J1	GND
5	Control Plane Port 2	SYS_CON*	GND	GND-J1	CP02-T0-	CP02-T0+	GND	GND-J1	CP02-R0-	CP02-R0+
6		GND	CP02-T1-	CP02-T1+	GND-J1	GND	CP02-R1-	CP02-R1+	GND-J1	GND
7		Reserved	GND	GND-J1	CP02-T2-	CP02-T2+	GND	GND-J1	CP02-R2-	CP02-R2+
8		GND	CP02-T3-	CP02-T3+	GND-J1	GND	CP02-R3-	CP02-R3+	GND-J1	GND
9	Control Plane Port 3	UD	GND	GND-J1	CP03-T0-	CP03-T0+	GND	GND-J1	CP03-R0-	CP03-R0+
10		GND	CP03-T1-	CP03-T1+	GND-J1	GND	CP03-R1-	CP03-R1+	GND-J1	GND
11		UD	GND	GND-J1	CP03-T2-	CP03-T2+	GND	GND-J1	CP03-R2-	CP03-R2+
12		GND	CP03-T3-	CP03-T3+	GND-J1	GND	CP03-R3-	CP03-R3+	GND-J1	GND
13	Control Plane Port 4	UD	GND	GND-J1	CP04-T0-	CP04-T0+	GND	GND-J1	CP04-R0-	CP04-R0+
14		GND	CP04-T1-	CP04-T1+	GND-J1	GND	CP04-R1-	CP04-R1+	GND-J1	GND
15		Maskable Reset*	GND	GND-J1	CP04-T2-	CP04-T2+	GND	GND-J1	CP04-R2-	CP04-R2+
16		GND	CP04-T3-	CP04-T3+	GND-J1	GND	CP04-R3-	CP04-R3+	GND-J1	GND

J2/P2 Signal Assignments for Switch Slot 6

Plug-In Module P2		Row G	Row F	Row E Even	Row E Odd	Row D	Row C	Row B Even	Row B Odd	Row A
Bplane J2		Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a
1	Control Plane Thin Pipes 1 - 8	UD	GND	GND-J2	CPtp01-DB-	CPtp01-DB+	GND	GND-J2	CPtp01-DA-	CPtp01-DA+
2		GND	CPtp01-DD-	CPtp01-DD+	GND-J2	GND	CPtp01-DC-	CPtp01-DC+	GND-J2	GND
3		UD	GND	GND-J2	CPtp02-DB-	CPtp02-DB+	GND	GND-J2	CPtp02-DA-	CPtp02-DA+
4		GND	CPtp02-DD-	CPtp02-DD+	GND-J2	GND	CPtp02-DC-	CPtp02-DC+	GND-J2	GND
5		UD	GND	GND-J2	CPtp03-DB-	CPtp03-DB+	GND	GND-J2	CPtp03-DA-	CPtp03-DA+
6		GND	CPtp03-DD-	CPtp03-DD+	GND-J2	GND	CPtp03-DC-	CPtp03-DC+	GND-J2	GND
7		UD	GND	GND-J2	CPtp04-DB-	CPtp04-DB+	GND	GND-J2	CPtp04-DA-	CPtp04-DA+
8		GND	CPtp04-DD-	CPtp04-DD+	GND-J2	GND	CPtp04-DC-	CPtp04-DC+	GND-J2	GND
9		UD	GND	GND-J2	CPtp05-DB-	CPtp05-DB+	GND	GND-J2	CPtp05-DA-	CPtp05-DA+
10		GND	CPtp05-DD-	CPtp05-DD+	GND-J2	GND	CPtp05-DC-	CPtp05-DC+	GND-J2	GND
11		UD	GND	GND-J2	CPtp06-DB-	CPtp06-DB+	GND	GND-J2	CPtp06-DA-	CPtp06-DA+
12		GND	CPtp06-DD-	CPtp06-DD+	GND-J2	GND	CPtp06-DC-	CPtp06-DC+	GND-J2	GND
13		UD	GND	GND-J2	CPtp07-DB-	CPtp07-DB+	GND	GND-J2	CPtp07-DA-	CPtp07-DA+
14		GND	CPtp07-DD-	CPtp07-DD+	GND-J2	GND	CPtp07-DC-	CPtp07-DC+	GND-J2	GND
15		UD	GND	GND-J2	CPtp08-DB-	CPtp08-DB+	GND	GND-J2	CPtp08-DA-	CPtp08-DA+
16		GND	CPtp08-DD-	CPtp08-DD+	GND-J2	GND	CPtp08-DC-	CPtp08-DC+	GND-J2	GND

J3/P3 Signal Assignments for Switch Slot 6

Plug-In Module P3		Row G	Row F	Row E Even	Row E Odd	Row D	Row C	Row B Even	Row B Odd	Row A
Bplane J3		Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a
1	Control Plane Thin Pipes 9 - 16	UD	GND	GND-J3	CPtp09-DB-	CPtp09-DB+	GND	GND-J3	CPtp09-DA-	CPtp09-DA+
2		GND	CPtp09-DD-	CPtp09-DD+	GND-J3	GND	CPtp09-DC-	CPtp09-DC+	GND-J3	GND
3		UD	GND	GND-J3	CPtp10-DB-	CPtp10-DB+	GND	GND-J3	CPtp10-DA-	CPtp10-DA+
4		GND	CPtp10-DD-	CPtp10-DD+	GND-J3	GND	CPtp10-DC-	CPtp10-DC+	GND-J3	GND
5		UD	GND	GND-J3	CPtp11-DB-	CPtp11-DB+	GND	GND-J3	CPtp11-DA-	CPtp11-DA+
6		GND	CPtp11-DD-	CPtp11-DD+	GND-J3	GND	CPtp11-DC-	CPtp11-DC+	GND-J3	GND
7		UD	GND	GND-J3	CPtp12-DB-	CPtp12-DB+	GND	GND-J3	CPtp12-DA-	CPtp12-DA+
8		GND	CPtp12-DD-	CPtp12-DD+	GND-J3	GND	CPtp12-DC-	CPtp12-DC+	GND-J3	GND
9		UD	GND	GND-J3	CPtp13-DB-	CPtp13-DB+	GND	GND-J3	CPtp13-DA-	CPtp13-DA+
10		GND	CPtp13-DD-	CPtp13-DD+	GND-J3	GND	CPtp13-DC-	CPtp13-DC+	GND-J3	GND
11		UD	GND	GND-J3	CPtp14-DB-	CPtp14-DB+	GND	GND-J3	CPtp14-DA-	CPtp14-DA+
12		GND	CPtp14-DD-	CPtp14-DD+	GND-J3	GND	CPtp14-DC-	CPtp14-DC+	GND-J3	GND
13		UD	GND	GND-J3	CPtp15-DB-	CPtp15-DB+	GND	GND-J3	CPtp15-DA-	CPtp15-DA+
14		GND	CPtp15-DD-	CPtp15-DD+	GND-J3	GND	CPtp15-DC-	CPtp15-DC+	GND-J3	GND
15		UD	GND	GND-J3	CPtp16-DB-	CPtp16-DB+	GND	GND-J3	CPtp16-DA-	CPtp16-DA+
16		GND	CPtp16-DD-	CPtp16-DD+	GND-J3	GND	CPtp16-DC-	CPtp16-DC+	GND-J3	GND

J4/P4 Signal Assignments for Switch Slot 6

Plug-In Module P4		Row G	Row F	Row E Even	Row E Odd	Row D	Row C	Row B Even	Row B Odd	Row A
Bplane J4		Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a
1	Control Plane Thin Pipes 17 - 24	UD	GND	GND-J4	CPtp17-DB-	CPtp17-DB+	GND	GND-J4	CPtp17-DA-	CPtp17-DA+
2		GND	CPtp17-DD-	CPtp17-DD+	GND-J3	GND	CPtp17-DC-	CPtp17-DC+	GND-J4	GND
3		UD	GND	GND-J4	CPtp18-DB-	CPtp18-DB+	GND	GND-J4	CPtp18-DA-	CPtp18-DA+
4		GND	CPtp18-DD-	CPtp18-DD+	GND-J4	GND	CPtp18-DC-	CPtp18-DC+	GND-J4	GND
5		UD	GND	GND-J4	CPtp19-DB-	CPtp19-DB+	GND	GND-J3	CPtp19-DA-	CPtp19-DA+
6		GND	CPtp19-DD-	CPtp19-DD+	GND-J4	GND	CPtp19-DC-	CPtp19-DC+	GND-J4	GND
7		UD	GND	GND-J4	CPtp20-DB-	CPtp20-DB+	GND	GND-J4	CPtp20-DA-	CPtp20-DA+
8		GND	CPtp20-DD-	CPtp20-DD+	GND-J4	GND	CPtp20-DC-	CPtp20-DC+	GND-J4	GND
9		UD	GND	GND-J4	CPtp21-DB-	CPtp21-DB+	GND	GND-J4	CPtp21-DA-	CPtp21-DA+
10		GND	CPtp21-DD-	CPtp21-DD+	GND-J4	GND	CPtp21-DC-	CPtp21-DC+	GND-J4	GND
11		UD	GND	GND-J4	CPtp22-DB-	CPtp22-DB+	GND	GND-J4	CPtp22-DA-	CPtp22-DA+
12		GND	CPtp22-DD-	CPtp22-DD+	GND-J4	GND	CPtp22-DC-	CPtp22-DC+	GND-J4	GND
13		UD	GND	GND-J4	CPtp23-DB-	CPtp23-DB+	GND	GND-J4	CPtp23-DA-	CPtp23-DA+
14		GND	CPtp23-DD-	CPtp23-DD+	GND-J4	GND	CPtp23-DC-	CPtp23-DC+	GND-J4	GND
15		UD	GND	GND-J4	CPtp24-DB-	CPtp24-DB+	GND	GND-J4	CPtp24-DA-	CPtp24-DA+
16		GND	CPtp24-DD-	CPtp24-DD+	GND-J4	GND	CPtp24-DC-	CPtp24-DC+	GND-J4	GND

J2-J6 slots 1-5 and J5, J6 Signal Assignments = User Defined

6U, 7-Slot Signal Assignments

J0 Signal Assignments

	Row A	Row B	Row C	Row D	Row E	Row F	Row G	Row H	Row I
1	Vs2	Vs2	Vs2	Vs2	[redacted]	Vs1	Vs1	Vs1	Vs1
2	Vs2	Vs2	Vs2	Vs2		Vs1	Vs1	Vs1	Vs1
3	Vs3	Vs3	Vs3	Vs3		Vs3	Vs3	Vs3	Vs3
4	GND	NVMRO	SYSRESET*	GND	-12V_Aux	GND	SM3	SM2	GND
5	GND	SM1	SM0	GND	3.3V_Aux	GND	GA4*	GAP*	GND
6	GND	GA0*	GA1*	GND	+12V_Aux	GND	GA2*	GA3*	GND
7	TRST*	TMS	GND	GND	TDI	TDO	GND	GND	TCK
8	GND	GND	AUX_CLK+	AUX_CLK-	GND	GND	REF_CLK+	REF_CLK-	GND

J2/P2 Signal Assignments for Slots 3&4

	Row I	Row H	Row G	Row F	Row E	Row D	Row C	Row B	Row A
1	GND	D08	ACFAIL*	GND	BBSY*	GND	SYSFAIL*	D00	GND
2	GND	D09	BG2IN*	GND	BCLR*	GND	BR0*	D01	GND
3	GND	D10	BG2OUT*	GND	BG0IN*	GND	BR1*	D02	GND
4	GND	D11	BG3IN*	GND	BG0OUT*	GND	BR2*	D03	GND
5	GND	D12	BG3OUT*	GND	BG1IN*	GND	BR3*	D04	GND
6	GND	D13	BERR*	GND	BG1OUT*	GND	AM0	D05	GND
7	GND	D14	LWORD*	GND	SYSCLK	GND	AM1	D06	GND
8	GND	D15	AM5	GND	DS1*	GND	AM2	D07	GND
9	GND	A22	A23	GND	DS0*	GND	AM3	AM4	GND
10	GND	A20	A21	GND	WRITE*	GND	IRQ7*	A07	GND
11	GND	A18	A19	GND	DTACK*	GND	IRQ6*	A06	GND
12	GND	A16	A17	GND	AS*	GND	IRQ5*	A05	GND
13	GND	A14	A15	GND	IACK*	GND	IRQ4*	A04	GND
14	GND	A12	A13	GND	IACKIN*	GND	IRQ3*	A03	GND
15	GND	A10	A11	GND	IACKOUT*	GND	IRQ2*	A02	GND
16	GND	A08	A09	GND	RETRY*	GND	IRQ1*	A01	GND

J3-J6 on slots 3 and 4 and J2-J6 on slots 5-7 = User Defined

J1/P1 Payload Signal Assignments for Slots 3-7

Plug-In Mod P4		Row G	Row F	Row E Even	Row E Odd	Row D	Row C	Row B Even	Row B Odd	Row A
Bplane J4		Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a
1	User Defined	UD	GND	GND-J4	UD	UD	GND	GND-J4	UD	UD
2		GND	UD	UD	GND-J4	GND	UD	UD	GND-J4	GND
3		UD	GND	GND-J4	UD	UD	GND	GND-J4	UD	UD
4		GND	UD	UD	GND-J4	GND	UD	UD	GND-J4	GND
5		UD	GND	GND-J4	UD	UD	GND	GND-J4	UD	UD
6		GND	UD	UD	GND-J4	GND	UD	UD	GND-J4	GND
7		UD	GND	GND-J4	UD	UD	GND	GND-J4	UD	UD
8		GND	UD	UD	GND-J4	GND	UD	UD	GND-J4	GND
9		UD	GND	GND-J4	UD	UD	GND	GND-J4	UD	UD
10		GND	UD	UD	GND-J4	GND	UD	UD	GND-J4	GND
11		UD	GND	GND-J4	UD	UD	GND	GND-J4	UD	UD
12		GND	UD	UD	GND-J4	GND	UD	UD	GND-J4	GND
13	Control Plane 2 TPs	UD	GND	GND-J4	CPtp02-DB-	CPtp02-DB+	GND	GND-J4	CPtp02-DA-	CPtp02-DA+
14		GND	CPtp02-DD-	CPtp02-DD+	GND-J4	GND	CPtp02-DC-	CPtp02-DC+	GND-J4	GND
15		UD	GND	GND-J4	CPtp01-DB-	CPtp01-DB+	GND	GND-J4	CPtp01-DA-	CPtp01-DA+
16		GND	CPtp01-DD-	CPtp01-DD+	GND-J4	GND	CPtp01-DC-	CPtp01-DC+	GND-J4	GND

6U, 9-Slot Signal Assignments

J0 Signal Assignments

	Row I	Row H	Row G	Row F	Row E	Row D	Row C	Row B	Row A
1	Vs1	Vs1	Vs1	Vs1	No Pad	Vs2	Vs2	Vs2	Vs2
2	Vs1	Vs1	Vs1	Vs1	No Pad	Vs2	Vs2	Vs2	Vs2
3	Vs3	Vs3	Vs3	Vs3	No Pad	Vs3	Vs3	Vs3	Vs3
4	GND	SM2	SM3	GND	-12V_Aux	GND	SYSRESET*	NVMRO	GND
5	GND	GAP*	GA4*	GND	3.3V_Aux	GND	SM0	SM1	GND
6	GND	GA3*	GA2*	GND	+12V_Aux	GND	GA1*	GA0*	GND
7	TCK	GND	GND	TDO	TDI	GND	GND	TMS	TRST*
8	GND	REF_CLK-	REF_CLK+	GND	GND	AUX_CLK-	AUX_CLK+	GND	GND

J1/P1 Payload Slot Signal Assignments

Plug-In Module P1		Row G	Row F	Row E Even	Row E Odd	Row D	Row C	Row B Even	Row B Odd	Row A
Bplane J1		Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a
1	Data Plane Port 1	GDiscrete1	GND	GND-J1	DP01-T0-	DP01-T0+	GND	GND-J1	DP01-R0-	DP01-R0+
2		GND	DP01-T1-	DP01-T1+	GND-J1	GND	DP01-R1-	DP01-R1+	GND-J1	GND
3		P1-VBAT	GND	GND-J1	DP01-T2-	DP01-T2+	GND	GND-J1	DP01-R2-	DP01-R2+
4		GND	DP01-T3-	DP01-T3+	GND-J1	GND	DP01-R3-	DP01-R3+	GND-J1	GND
5	Data Plane Port 2	SYS_CON*	GND	GND-J1	DP02-T0-	DP02-T0+	GND	GND-J1	DP02-R0-	DP02-R0+
6		GND	DP02-T1-	DP02-T1+	GND-J1	GND	DP02-R1-	DP02-R1+	GND-J1	GND
7		Reserved	GND	GND-J1	DP02-T2-	DP02-T2+	GND	GND-J1	DP02-R2-	DP02-R2+
8		GND	DP02-T3-	DP02-T3+	GND-J1	GND	DP02-R3-	DP02-R3+	GND-J1	GND
9	Data Plane Port 3	UD	GND	GND-J1	DP03-T0-	DP03-T0+	GND	GND-J1	DP03-R0-	DP03-R0+
10		GND	DP03-T1-	DP03-T1+	GND-J1	GND	DP03-R1-	DP03-R1+	GND-J1	GND
11		UD	GND	GND-J1	DP03-T2-	DP03-T2+	GND	GND-J1	DP03-R2-	DP03-R2+
12		GND	DP03-T3-	DP03-T3+	GND-J1	GND	DP03-R3-	DP03-R3+	GND-J1	GND
13	Data Plane Port 4	UD	GND	GND-J1	DP04-T0-	DP04-T0+	GND	GND-J1	DP04-R0-	DP04-R0+
14		GND	DP04-T1-	DP04-T1+	GND-J1	GND	DP04-R1-	DP04-R1+	GND-J1	GND
15		Maskable Reset*	GND	GND-J1	DP04-T2-	DP04-T2+	GND	GND-J1	DP04-R2-	DP04-R2+
16		GND	DP04-T3-	DP04-T3+	GND-J1	GND	DP04-R3-	DP04-R3+	GND-J1	GND

J2/P2 Payload Slot Signal Assignments

Plug-In Module P2		Row G	Row F	Row E Even	Row E Odd	Row D	Row C	Row B Even	Row B Odd	Row A
Bplane J2		Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a
1	Data Plane Port 5	UD	GND	GND-J2	DP05-T0-	DP05-T0+	GND	GND-J2	DP05-R0-	DP05-R0+
2		GND	DP05-T1-	DP05-T1+	GND-J2	GND	DP05-R1-	DP05-R1+	GND-J2	GND
3		UD	GND	GND-J2	DP05-T2-	DP05-T2+	GND	GND-J2	DP05-R2-	DP05-R2+
4		GND	DP05-T3-	DP05-T3+	GND-J2	GND	DP05-R3-	DP05-R3+	GND-J2	GND
5	Data Plane Port 6	UD	GND	GND-J2	DP06-T0-	DP06-T0+	GND	GND-J2	DP06-R0-	DP06-R0+
6		GND	DP06-T1-	DP06-T1+	GND-J2	GND	DP06-R1-	DP06-R1+	GND-J2	GND
7		UD	GND	GND-J2	DP06-T2-	DP06-T2+	GND	GND-J2	DP06-R2-	DP06-R2+
8		GND	DP06-T3-	DP06-T3+	GND-J2	GND	DP06-R3-	DP06-R3+	GND-J2	GND
9	Data Plane Port 7	UD	GND	GND-J2	DP07-T0-	DP07-T0+	GND	GND-J2	DP07-R0-	DP07-R0+
10		GND	DP07-T1-	DP07-T1+	GND-J2	GND	DP07-R1-	DP07-R1+	GND-J2	GND
11		UD	GND	GND-J2	DP07-T2-	DP07-T2+	GND	GND-J2	DP07-R2-	DP07-R2+
12		GND	DP07-T3-	DP07-T3+	GND-J2	GND	DP07-R3-	DP07-R3+	GND-J2	GND
13	Data Plane Port 8	UD	GND	GND-J2	DP08-T0-	DP08-T0+	GND	GND-J2	DP08-R0-	DP08-R0+
14		GND	DP08-T1-	DP08-T1+	GND-J2	GND	DP08-R1-	DP08-R1+	GND-J2	GND
15		UD	GND	GND-J2	DP08-T2-	DP08-T2+	GND	GND-J2	DP08-R2-	DP08-R2+
16		GND	DP08-T3-	DP08-T3+	GND-J2	GND	DP08-R3-	DP08-R3+	GND-J2	GND

J3, J5-J6 Payload Signal Assignments = User Defined

J4/P4 Payload Slot Signal Assignments

Plug-In Mod P4		Row G	Row F	Row E Even	Row E Odd	Row D	Row C	Row B Even	Row B Odd	Row A
Bplane J4		Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a
1	User Defined	UD	GND	GND-J4	UD	UD	GND	GND-J4	UD	UD
2		GND	UD	UD	GND-J4	GND	UD	UD	GND-J4	GND
3		UD	GND	GND-J4	UD	UD	GND	GND-J4	UD	UD
4		GND	UD	UD	GND-J4	GND	UD	UD	GND-J4	GND
5		UD	GND	GND-J4	UD	UD	GND	GND-J4	UD	UD
6		GND	UD	UD	GND-J4	GND	UD	UD	GND-J4	GND
7		UD	GND	GND-J4	UD	UD	GND	GND-J4	UD	UD
8		GND	UD	UD	GND-J4	GND	UD	UD	GND-J4	GND
9		UD	GND	GND-J4	UD	UD	GND	GND-J4	UD	UD
10		GND	UD	UD	GND-J4	GND	UD	UD	GND-J4	GND
11	RSVD	UD	GND	GND-J4	RSVD	RSVD	GND	GND-J4	RSVD	RSVD
12		GND	RSVD	RSVD	GND-J4	GND	RSVD	RSVD	GND-J4	GND
13	User Defined	UD	GND	GND-J4	UD	UD	GND	GND-J4	UD	UD
14		GND	UD	UD	GND-J4	GND	UD	UD	GND-J4	GND
15		UD	GND	GND-J4	UD	UD	GND	GND-J4	UD	UD
16		GND	UD	UD	GND-J4	GND	UD	UD	GND-J4	GND

J1/P1 Switch Slot Signal Assignments

Plug-In Module P1		Row G	Row F	Row E Even	Row E Odd	Row D	Row C	Row B Even	Row B Odd	Row A
Bplane J1		Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a
1	Data Plane Port 1	GDiscrete1	GND	GND-J1	DP01-T0-	DP01-T0+	GND	GND-J1	DP01-R0-	DP01-R0+
2		GND	DP01-T1-	DP01-T1+	GND-J1	GND	DP01-R1-	DP01-R1+	GND-J1	GND
3		P1-VBAT	GND	GND-J1	DP01-T2-	DP01-T2+	GND	GND-J1	DP01-R2-	DP01-R2+
4		GND	DP01-T3-	DP01-T3+	GND-J1	GND	DP01-R3-	DP01-R3+	GND-J1	GND
5	Data Plane Port 2	SYS_CON*	GND	GND-J1	DP02-T0-	DP02-T0+	GND	GND-J1	DP02-R0-	DP02-R0+
6		GND	DP02-T1-	DP02-T1+	GND-J1	GND	DP02-R1-	DP02-R1+	GND-J1	GND
7		Reserved	GND	GND-J1	DP02-T2-	DP02-T2+	GND	GND-J1	DP02-R2-	DP02-R2+
8		GND	DP02-T3-	DP02-T3+	GND-J1	GND	DP02-R3-	DP02-R3+	GND-J1	GND
9	User Defined	UD	GND	GND-J1	UD	UD	GND	GND-J1	UD	UD
10		GND	UD	UD	GND-J1	GND	UD	UD	GND-J1	GND
11		UD	GND	GND-J1	UD	UD	GND	GND-J1	UD	UD
12		GND	UD	UD	GND-J1	GND	UD	UD	GND-J1	GND
13		UD	GND	GND-J1	UD	UD	GND	GND-J1	UD	UD
14		GND	UD	UD	GND-J1	GND	UD	UD	GND-J1	GND
15		Maskable Reset*	GND	GND-J1	UD	UD	GND	GND-J1	UD	UD
16		GND	UD	UD	GND-J1	GND	UD	UD	GND-J1	GND

J2-J6 Switch Signal Assignments = User Defined

OpenVPX Backplanes - Signal Assignments

6U, 10-Slot Signal Assignments

J0 Signal Assignments

	Row I	Row H	Row G	Row F	Row E	Row D	Row C	Row B	Row A
1	Vs1	Vs1	Vs1	Vs1	No Pad	Vs2	Vs2	Vs2	Vs2
2	Vs1	Vs1	Vs1	Vs1	No Pad	Vs2	Vs2	Vs2	Vs2
3	Vs3	Vs3	Vs3	Vs3	No Pad	Vs3	Vs3	Vs3	Vs3
4	GND	SM2	SM3	GND	-12V_Aux	GND	SYSRESET*	NVMRO	GND
5	GND	GAP*	GA4*	GND	3.3V_Aux	GND	SM0	SM1	GND
6	GND	GA3*	GA2*	GND	+12V_Aux	GND	GA1*	GA0*	GND
7	TCK	GND	GND	TDO	TDI	GND	GND	TMS	TRST*
8	GND	REF_CLK-	REF_CLK+	GND	GND	AUX_CLK-	AUX_CLK+	GND	GND

J1/P1 Payload Slot Signal Assignments

Plug-In Module P1		Row G	Row F	Row E		Row D	Row C	Row B		Row A
				Even	Odd			Even	Odd	
Bplane J1		Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a
1	Data Plane Port 1	GDiscrete1	GND	GND-J1	DP01-T0-	DP01-T0+	GND	GND-J1	DP01-R0-	DP01-R0+
2		GND	DP01-T1-	DP01-T1+	GND-J1	GND	DP01-R1-	DP01-R1+	GND-J1	GND
3		P1-VBAT	GND	GND-J1	DP01-T2-	DP01-T2+	GND	GND-J1	DP01-R2-	DP01-R2+
4		GND	DP01-T3-	DP01-T3+	GND-J1	GND	DP01-R3-	DP01-R3+	GND-J1	GND
5	Data Plane Port 2	SYS_CON*	GND	GND-J1	DP02-T0-	DP02-T0+	GND	GND-J1	DP02-R0-	DP02-R0+
6		GND	DP02-T1-	DP02-T1+	GND-J1	GND	DP02-R1-	DP02-R1+	GND-J1	GND
7		Reserved	GND	GND-J1	DP02-T2-	DP02-T2+	GND	GND-J1	DP02-R2-	DP02-R2+
8		GND	DP02-T3-	DP02-T3+	GND-J1	GND	DP02-R3-	DP02-R3+	GND-J1	GND
9	Data Plane Port 3	UD	GND	GND-J1	DP03-T0-	DP03-T0+	GND	GND-J1	DP03-R0-	DP03-R0+
10		GND	DP03-T1-	DP03-T1+	GND-J1	GND	DP03-R1-	DP03-R1+	GND-J1	GND
11		UD	GND	GND-J1	DP03-T2-	DP03-T2+	GND	GND-J1	DP03-R2-	DP03-R2+
12		GND	DP03-T3-	DP03-T3+	GND-J1	GND	DP03-R3-	DP03-R3+	GND-J1	GND
13	Data Plane Port 4	UD	GND	GND-J1	DP04-T0-	DP04-T0+	GND	GND-J1	DP04-R0-	DP04-R0+
14		GND	DP04-T1-	DP04-T1+	GND-J1	GND	DP04-R1-	DP04-R1+	GND-J1	GND
15		Maskable Reset*	GND	GND-J1	DP04-T2-	DP04-T2+	GND	GND-J1	DP04-R2-	DP04-R2+
16		GND	DP04-T3-	DP04-T3+	GND-J1	GND	DP04-R3-	DP04-R3+	GND-J1	GND

J2/P2 Payload Slot Signal Assignments

Plug-In Module P2				Row G	Row F	Row E		Row D	Row C	Row B		Row A
						Even	Odd			Even	Odd	
Backplane J2				Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a
1	X16 using [15:0]	x8 using [7:0]	x4 using [3:0]	UD	GND	GND-J2	EP00-T-	EP00-T+	GND	GND-J2	EP00-R-	EP00-R+
2				GND	EP01-T-	EP01-T+	GND-J2	GND	EP01-R-	EP01-R+	GND-J2	GND
3				UD	GND	GND-J2	EP02-T-	EP02-T+	GND	GND-J2	EP02-R-	EP02-R+
4				GND	EP03-T-	EP03-T+	GND-J2	GND	EP03-R-	EP03-R+	GND-J2	GND
5			x4 using [7:4]	UD	GND	GND-J2	EP04-T-	EP04-T+	GND	GND-J2	EP04-R-	EP04-R+
6				GND	EP05-T-	EP05-T+	GND-J2	GND	EP05-R-	EP05-R+	GND-J2	GND
7				UD	GND	GND-J2	EP06-T-	EP06-T+	GND	GND-J2	EP06-R-	EP06-R+
8				GND	EP07-T-	EP07-T+	GND-J2	GND	EP07-R-	EP07-R+	GND-J2	GND
9		x8 using[15:8]	x4 using [11:8]	UD	GND	GND-J2	EP08-T-	EP08-T+	GND	GND-J2	EP08-R-	EP08-R+
10				GND	EP09-T-	EP09-T+	GND-J2	GND	EP09-R-	EP09-R+	GND-J2	GND
11				UD	GND	GND-J2	EP10-T-	EP10-T+	GND	GND-J2	EP10-R-	EP10-R+
12				GND	EP11-T-	EP11-T+	GND-J2	GND	EP11-R-	EP11-R+	GND-J2	GND
13			x4 using[15:12]	UD	GND	GND-J2	EP12-T-	EP12-T+	GND	GND-J2	EP12-R-	EP12-R+
14				GND	EP13-T-	EP13-T+	GND-J2	GND	EP13-R-	EP13-R+	GND-J2	GND
15				UD	GND	GND-J2	EP14-T-	EP14-T+	GND	GND-J2	EP14-R-	EP14-R+
16				GND	EP15-T-	EP15-T+	GND-J2	GND	EP15-R-	EP15-R+	GND-J2	GND

J3, J5-J6 Payload Signal Assignments = User Defined

J4/P4 Payload Slot Signal Assignments

Plug-In Mod P4		Row G	Row F	Row E		Row D	Row C	Row B		Row A
				Even	Odd			Even	Odd	
Bplane J4		Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a
1	User Defined	UD	GND	GND-J4	UD	UD	GND	GND-J4	UD	UD
2		GND	UD	UD	GND-J4	GND	UD	UD	GND-J4	GND
3		UD	GND	GND-J4	UD	UD	GND	GND-J4	UD	UD
4		GND	UD	UD	GND-J4	GND	UD	UD	GND-J4	GND
5		UD	GND	GND-J4	UD	UD	GND	GND-J4	UD	UD
6		GND	UD	UD	GND-J4	GND	UD	UD	GND-J4	GND
7		UD	GND	GND-J4	UD	UD	GND	GND-J4	UD	UD
8		GND	UD	UD	GND-J4	GND	UD	UD	GND-J4	GND
9		UD	GND	GND-J4	UD	UD	GND	GND-J4	UD	UD
10		GND	UD	UD	GND-J4	GND	UD	UD	GND-J4	GND
11	2 UTP	UD	GND	GND-J4	CPutp02-T-	CPutp02-T+	GND	GND-J4	CPutp02-R-	CPutp02-R+
12		GND	CPutp01-T-	CPutp01-T+	GND-J4	GND	CPutp01-R-	CPutp01-R+	GND-J4	GND
13	Control Plane 2 TPs	UD	GND	GND-J4	CPtp02-DB-	CPtp02-DB+	GND	GND-J4	CPtp02-DA-	CPtp02-DA+
14		GND	CPtp02-DD-	CPtp02-DD+	GND-J4	GND	CPtp02-DC-	CPtp02-DC+	GND-J4	GND
15		UD	GND	GND-J4	CPtp01-DB-	CPtp01-DB+	GND	GND-J4	CPtp01-DA-	CPtp01-DA+
16		GND	CPtp01-DD-	CPtp01-DD+	GND-J4	GND	CPtp01-DC-	CPtp01-DC+	GND-J4	GND

J1/P1 Switch Slot Signal Assignments

Plug-In Module P1		Row G	Row F	Row E		Row D	Row C	Row B		Row A
				Even	Odd			Even	Odd	
Bplane J1		Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a
1	CPlane Inter-SW UTPs Ports 1 - 4	GDiscrete1	GND	GND-J1	CSutp01-T-	CSutp01-T+	GND	GND-J1	CSutp01-R-	CSutp01-R+
2		GND	CSutp02-T-	CSutp02-T+	GND-J1	GND	CSutp02-R-	CSutp02-R+	GND-J1	GND
3		P1-VBAT	GND	GND-J1	CSutp03-T-	CSutp03-T+	GND	GND-J1	CSutp03-R-	CSutp03-R+
4		GND	CSutp04-T-	CSutp04-T+	GND-J1	GND	CSutp04-R-	CSutp04-R+	GND-J1	GND
5	Control Plane Payload UTPs Ports 1 - 12	SYS_CON*	GND	GND-J1	CPutp01-T-	CPutp01-T+	GND	GND-J1	CPutp01-R-	CPutp01-R+
6		GND	CPutp02-T-	CPutp02-T+	GND-J1	GND	CPutp02-R-	CPutp02-R+	GND-J1	GND
7		Reserved	GND	GND-J1	CPutp03-T-	CPutp03-T+	GND	GND-J1	CPutp03-R-	CPutp03-R+
8		GND	CPutp04-T-	CPutp04-T+	GND-J1	GND	CPutp04-R-	CPutp04-R+	GND-J1	GND
9		UD	GND	GND-J1	CPutp05-T-	CPutp05-T+	GND	GND-J1	CPutp05-R-	CPutp05-R+
10		GND	CPutp06-T-	CPutp06-T+	GND-J1	GND	CPutp06-R-	CPutp06-R+	GND-J1	GND
11		UD	GND	GND-J1	CPutp07-T-	CPutp07-T+	GND	GND-J1	CPutp07-R-	CPutp07-R+
12		GND	CPutp08-T-	CPutp08-T+	GND-J1	GND	CPutp08-R-	CPutp08-R+	GND-J1	GND
13		UD	GND	GND-J1	CPutp09-T-	CPutp09-T+	GND	GND-J1	CPutp09-R-	CPutp09-R+
14		GND	CPutp10-T-	CPutp10-T+	GND-J1	GND	CPutp10-R-	CPutp10-R+	GND-J1	GND
15		Maskable Reset*	GND	GND-J1	CPutp11-T-	CPutp11-T+	GND	GND-J1	CPutp11-R-	CPutp11-R+
16		GND	CPutp12-T-	CPutp12-T+	GND-J1	GND	CPutp12-R-	CPutp12-R+	GND-J1	GND

J2/P2 Switch Slot Signal Assignments

Plug-In Module P2		Row G	Row F	Row E		Row D	Row C	Row B		Row A
				Even	Odd			Even	Odd	
Bplane J2		Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a
1	Data Plane FP Port 16	UD	GND	GND-J2	DP16-T0-	DP16-T0+	GND	GND-J2	DP16-R0-	DP16-R0+
2		GND	DP16-T1-	DP16-T1+	GND-J2	GND	DP16-R1-	DP16-R1+	GND-J2	GND
3		UD	GND	GND-J2	DP16-T2-	DP16-T2+	GND	GND-J2	DP16-R2-	DP16-R2+
4		GND	DP16-T3-	DP16-T3+	GND-J2	GND	DP16-R3-	DP16-R3+	GND-J2	GND
5	Data Plane FP Port 15	UD	GND	GND-J2	DP15-T0-	DP15-T0+	GND	GND-J2	DP15-R0-	DP15-R0+
6		GND	DP15-T1-	DP15-T1+	GND-J2	GND	DP15-R1-	DP15-R1+	GND-J2	GND
7		UD	GND	GND-J2	DP15-T2-	DP15-T2+	GND	GND-J2	DP15-R2-	DP15-R2+
8		GND	DP15-T3-	DP15-T3+	GND-J2	GND	DP15-R3-	DP15-R3+	GND-J2	GND
9	Data Plane FP Port 14	UD	GND	GND-J2	DP14-T0-	DP14-T0+	GND	GND-J2	DP14-R0-	DP14-R0+
10		GND	DP14-T1-	DP14-T1+	GND-J2	GND	DP14-R1-	DP14-R1+	GND-J2	GND
11		UD	GND	GND-J2	DP14-T2-	DP14-T2+	GND	GND-J2	DP14-R2-	DP14-R2+
12		GND	DP14-T3-	DP14-T3+	GND-J2	GND	DP14-R3-	DP14-R3+	GND-J2	GND
13	Data Plane FP Port 13	UD	GND	GND-J2	DP13-T0-	DP13-T0+	GND	GND-J2	DP13-R0-	DP13-R0+
14		GND	DP13-T1-	DP13-T1+	GND-J2	GND	DP13-R1-	DP13-R1+	GND-J2	GND
15		UD	GND	GND-J2	DP13-T2-	DP13-T2+	GND	GND-J2	DP13-R2-	DP13-R2+
16		GND	DP13-T3-	DP13-T3+	GND-J2	GND	DP13-R3-	DP13-R3+	GND-J2	GND

J3/P3 Switch Slot Signal Assignments

Plug-In Module P2				Row G	Row F	Row E		Row D	Row C	Row B		Row A
						Even	Odd			Even	Odd	
Backplane J2				Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a
1	X16 using [15:0]	x8 using [7:0]	x4 using [3:0]	UD	GND	GND-J2	EP00-T-	EP00-T+	GND	GND-J2	EP00-R-	EP00-R+
2				GND	EP01-T-	EP01-T+	GND-J2	GND	EP01-R-	EP01-R+	GND-J2	GND
3				UD	GND	GND-J2	EP02-T-	EP02-T+	GND	GND-J2	EP02-R-	EP02-R+
4				GND	EP03-T-	EP03-T+	GND-J2	GND	EP03-R-	EP03-R+	GND-J2	GND
5			x4 using [7:4]	UD	GND	GND-J2	EP04-T-	EP04-T+	GND	GND-J2	EP04-R-	EP04-R+
6				GND	EP05-T-	EP05-T+	GND-J2	GND	EP05-R-	EP05-R+	GND-J2	GND
7				UD	GND	GND-J2	EP06-T-	EP06-T+	GND	GND-J2	EP06-R-	EP06-R+
8				GND	EP07-T-	EP07-T+	GND-J2	GND	EP07-R-	EP07-R+	GND-J2	GND
9		x8 using[15:8]	x4 using [11:8]	UD	GND	GND-J2	EP08-T-	EP08-T+	GND	GND-J2	EP08-R-	EP08-R+
10				GND	EP09-T-	EP09-T+	GND-J2	GND	EP09-R-	EP09-R+	GND-J2	GND
11				UD	GND	GND-J2	EP10-T-	EP10-T+	GND	GND-J2	EP10-R-	EP10-R+
12				GND	EP11-T-	EP11-T+	GND-J2	GND	EP11-R-	EP11-R+	GND-J2	GND
13			x4 using[15:12]	UD	GND	GND-J2	EP12-T-	EP12-T+	GND	GND-J2	EP12-R-	EP12-R+
14				GND	EP13-T-	EP13-T+	GND-J2	GND	EP13-R-	EP13-R+	GND-J2	GND
15				UD	GND	GND-J2	EP14-T-	EP14-T+	GND	GND-J2	EP14-R-	EP14-R+
16				GND	EP15-T-	EP15-T+	GND-J2	GND	EP15-R-	EP15-R+	GND-J2	GND

J4/P4 Switch Slot Signal Assignments

Plug-in Module P4		Row G	Row F	Row E		Row D	Row C	Row B		Row A
Bplane J4		Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a
1	Data Plane Payload FP Port 8	UD	GND	GND-J4	DP08-T0-	DP08-T0+	GND	GND-J4	DP08-R0-	DP08-R0+
2		GND	DP08-T1-	DP08-T1+	GND-J4	GND	DP08-R1-	DP08-R1+	GND-J4	GND
3		UD	GND	GND-J4	DP08-T2-	DP08-T2+	GND	GND-J4	DP08-R2-	DP08-R2+
4		GND	DP08-T3-	DP08-T3+	GND-J4	GND	DP08-R3-	DP08-R3+	GND-J4	GND
5	Data Plane Payload FP Port 7	UD	GND	GND-J4	DP07-T0-	DP07-T0+	GND	GND-J4	DP07-R0-	DP07-R0+
6		GND	DP07-T1-	DP07-T1+	GND-J4	GND	DP07-R1-	DP07-R1+	GND-J4	GND
7		UD	GND	GND-J4	DP07-T2-	DP07-T2+	GND	GND-J4	DP07-R2-	DP07-R2+
8		GND	DP07-T3-	DP07-T3+	GND-J4	GND	DP07-R3-	DP07-R3+	GND-J4	GND
9	Data Plane Payload FP Port 6	UD	GND	GND-J4	DP06-T0-	DP06-T0+	GND	GND-J4	DP06-R0-	DP06-R0+
10		GND	DP06-T1-	DP06-T1+	GND-J4	GND	DP06-R1-	DP06-R1+	GND-J4	GND
11		UD	GND	GND-J4	DP06-T2-	DP06-T2+	GND	GND-J4	DP06-R2-	DP06-R2+
12		GND	DP06-T3-	DP06-T3+	GND-J4	GND	DP06-R3-	DP06-R3+	GND-J4	GND
13	Data Plane Payload FP Port 5	UD	GND	GND-J4	DP05-T0-	DP05-T0+	GND	GND-J4	DP05-R0-	DP05-R0+
14		GND	DP05-T1-	DP05-T1+	GND-J4	GND	DP05-R1-	DP05-R1+	GND-J4	GND
15		UD	GND	GND-J4	DP05-T2-	DP05-T2+	GND	GND-J4	DP05-R2-	DP05-R2+
16		GND	DP05-T3-	DP05-T3+	GND-J4	GND	DP05-R3-	DP05-R3+	GND-J4	GND

J5/P5 Switch Slot Signal Assignments

Plug-In Module P5		Row G	Row F	Row E		Row D	Row C	Row B		Row A
Bplane J5		Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a
1	Data Plane Payload FP Port 4	UD	GND	GND-J5	DP04-T0-	DP04-T0+	GND	GND-J5	DP04-R0-	DP04-R0+
2		GND	DP04-T1-	DP04-T1+	GND-J5	GND	DP04-R1-	DP04-R1+	GND-J5	GND
3		UD	GND	GND-J5	DP04-T2-	DP04-T2+	GND	GND-J5	DP04-R2-	DP04-R2+
4		GND	DP04-T3-	DP04-T3+	GND-J5	GND	DP04-R3-	DP04-R3+	GND-J5	GND
5	Data Plane Payload FP Port 3	UD	GND	GND-J5	DP03-T0-	DP03-T0+	GND	GND-J5	DP03-R0-	DP03-R0+
6		GND	DP03-T1-	DP03-T1+	GND-J5	GND	DP03-R1-	DP03-R1+	GND-J5	GND
7		UD	GND	GND-J5	DP03-T2-	DP03-T2+	GND	GND-J5	DP03-R2-	DP03-R2+
8		GND	DP03-T3-	DP03-T3+	GND-J5	GND	DP03-R3-	DP03-R3+	GND-J5	GND
9	Data Plane Payload FP Port 2	UD	GND	GND-J5	DP02-T0-	DP02-T0+	GND	GND-J5	DP02-R0-	DP02-R0+
10		GND	DP02-T1-	DP02-T1+	GND-J5	GND	DP02-R1-	DP02-R1+	GND-J5	GND
11		UD	GND	GND-J5	DP02-T2-	DP02-T2+	GND	GND-J5	DP02-R2-	DP02-R2+
12		GND	DP02-T3-	DP02-T3+	GND-J5	GND	DP02-R3-	DP02-R3+	GND-J5	GND
13	Data Plane Payload FP Port 1	UD	GND	GND-J5	DP01-T0-	DP01-T0+	GND	GND-J5	DP01-R0-	DP01-R0+
14		GND	DP01-T1-	DP01-T1+	GND-J5	GND	DP01-R1-	DP01-R1+	GND-J5	GND
15		UD	GND	GND-J5	DP01-T2-	DP01-T2+	GND	GND-J5	DP01-R2-	DP01-R2+
16		GND	DP01-T3-	DP01-T3+	GND-J5	GND	DP01-R3-	DP01-R3+	GND-J5	GND

J6/P6 Switch Slot Signal Assignments

Plug-In Module P6		Row G	Row F	Row E		Row D	Row C	Row B		Row A
				Even	Odd			Even	Odd	
Bplane J6		Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a
1	Data Plane Inter-SW FP Port 4	UD	GND	GND-J6	DS04-T0-	DS04-T0+	GND	GND-J6	DS04-R0-	DS04-R0+
2		GND	DS04-T1-	DS04-T1+	GND-J6	GND	DS04-R1-	DS04-R1+	GND-J6	GND
3		UD	GND	GND-J6	DS04-T2-	DS04-T2+	GND	GND-J6	DS04-R2-	DS04-R2+
4		GND	DS04-T3-	DS04-T3+	GND-J6	GND	DS04-R3-	DS04-R3+	GND-J6	GND
5	Data Plane Inter-SW FP Port 3	UD	GND	GND-J6	DS03-T0-	DS03-T0+	GND	GND-J6	DS03-R0-	DS03-R0+
6		GND	DS03-T1-	DS03-T1+	GND-J6	GND	DS03-R1-	DS03-R1+	GND-J6	GND
7		UD	GND	GND-J6	DS03-T2-	DS03-T2+	GND	GND-J6	DS03-R2-	DS03-R2+
8		GND	DS03-T3-	DS03-T3+	GND-J6	GND	DS03-R3-	DS03-R3+	GND-J6	GND
9	Data Plane Inter-SW FP Port 2	UD	GND	GND-J6	DS02-T0-	DS02-T0+	GND	GND-J6	DS02-R0-	DS02-R0+
10		GND	DS02-T1-	DS02-T1+	GND-J6	GND	DS02-R1-	DS02-R1+	GND-J6	GND
11		UD	GND	GND-J6	DS02-T2-	DS02-T2+	GND	GND-J6	DS02-R2-	DS02-R2+
12		GND	DS02-T3-	DS02-T3+	GND-J6	GND	DS02-R3-	DS02-R3+	GND-J6	GND
13	Data Plane Inter-SW FP Port 1	UD	GND	GND-J6	DS01-T0-	DS01-T0+	GND	GND-J6	DS01-R0-	DS01-R0+
14		GND	DS01-T1-	DS01-T1+	GND-J6	GND	DS01-R1-	DS01-R1+	GND-J6	GND
15		UD	GND	GND-J6	DS01-T2-	DS01-T2+	GND	GND-J6	DS01-R2-	DS01-R2+
16		GND	DS01-T3-	DS01-T3+	GND-J6	GND	DS01-R3-	DS01-R3+	GND-J6	GND

6U, 16-Slot Signal Assignments

J0 Signal Assignments

	Row I	Row H	Row G	Row F	Row E	Row D	Row C	Row B	Row A
1	Vs1	Vs1	Vs1	Vs1	No Pad	Vs2	Vs2	Vs2	Vs2
2	Vs1	Vs1	Vs1	Vs1	No Pad	Vs2	Vs2	Vs2	Vs2
3	Vs3	Vs3	Vs3	Vs3	No Pad	Vs3	Vs3	Vs3	Vs3
4	GND	SM2	SM3	GND	-12V_Aux	GND	SYSRESET*	NVMRO	GND
5	GND	GAP*	GA4*	GND	3.3V_Aux	GND	SM0	SM1	GND
6	GND	GA3*	GA2*	GND	+12V_Aux	GND	GA1*	GA0*	GND
7	TCK	GND	GND	TDO	TDI	GND	GND	TMS	TRST*
8	GND	REF_CLK-	REF_CLK+	GND	GND	AUX_CLK-	AUX_CLK+	GND	GND

J1/P1 Payload Slot Signal Assignments

Plug-in Module P1		Row G	Row F	Row E		Row D	Row C	Row B		Row A
				Even	Odd			Even	Odd	
Bplane J1		Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a
1	Data Plane Port 1	GDiscrete1	GND	GND-J1	DP01-T0-	DP01-T0+	GND	GND-J1	DP01-R0-	DP01-R0+
2		GND	DP01-T1-	DP01-T1+	GND-J1	GND	DP01-R1-	DP01-R1+	GND-J1	GND
3		P1-VBAT	GND	GND-J1	DP01-T2-	DP01-T2+	GND	GND-J1	DP01-R2-	DP01-R2+
4		GND	DP01-T3-	DP01-T3+	GND-J1	GND	DP01-R3-	DP01-R3+	GND-J1	GND
5	Data Plane Port 2	SYS_CON*	GND	GND-J1	DP02-T0-	DP02-T0+	GND	GND-J1	DP02-R0-	DP02-R0+
6		GND	DP02-T1-	DP02-T1+	GND-J1	GND	DP02-R1-	DP02-R1+	GND-J1	GND
7		Reserved	GND	GND-J1	DP02-T2-	DP02-T2+	GND	GND-J1	DP02-R2-	DP02-R2+
8		GND	DP02-T3-	DP02-T3+	GND-J1	GND	DP02-R3-	DP02-R3+	GND-J1	GND
9	Data Plane Port 3	UD	GND	GND-J1	DP03-T0-	DP03-T0+	GND	GND-J1	DP03-R0-	DP03-R0+
10		GND	DP03-T1-	DP03-T1+	GND-J1	GND	DP03-R1-	DP03-R1+	GND-J1	GND
11		UD	GND	GND-J1	DP03-T2-	DP03-T2+	GND	GND-J1	DP03-R2-	DP03-R2+
12		GND	DP03-T3-	DP03-T3+	GND-J1	GND	DP03-R3-	DP03-R3+	GND-J1	GND
13	Data Plane Port 4	UD	GND	GND-J1	DP04-T0-	DP04-T0+	GND	GND-J1	DP04-R0-	DP04-R0+
14		GND	DP04-T1-	DP04-T1+	GND-J1	GND	DP04-R1-	DP04-R1+	GND-J1	GND
15		Maskable Reset*	GND	GND-J1	DP04-T2-	DP04-T2+	GND	GND-J1	DP04-R2-	DP04-R2+
16		GND	DP04-T3-	DP04-T3+	GND-J1	GND	DP04-R3-	DP04-R3+	GND-J1	GND

J4/P4 Payload Slot Signal Assignments

Plug-in Mod P4		Row G	Row F	Row E		Row D	Row C	Row B		Row A
				Even	Odd			Even	Odd	
Bplane J4		Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a
1	User Defined	UD	GND	GND-J4	UD	UD	GND	GND-J4	UD	UD
2		GND	UD	UD	GND-J4	GND	UD	UD	GND-J4	GND
3		UD	GND	GND-J4	UD	UD	GND	GND-J4	UD	UD
4		GND	UD	UD	GND-J4	GND	UD	UD	GND-J4	GND
5		UD	GND	GND-J4	UD	UD	GND	GND-J4	UD	UD
6		GND	UD	UD	GND-J4	GND	UD	UD	GND-J4	GND
7		UD	GND	GND-J4	UD	UD	GND	GND-J4	UD	UD
8		GND	UD	UD	GND-J4	GND	UD	UD	GND-J4	GND
9		UD	GND	GND-J4	UD	UD	GND	GND-J4	UD	UD
10		GND	UD	UD	GND-J4	GND	UD	UD	GND-J4	GND
11	2 UTP	UD	GND	GND-J4	CPutp02-T-	CPutp02-T+	GND	GND-J4	CPutp02-R-	CPutp02-R+
12		GND	CPutp01-T-	CPutp01-T+	GND-J4	GND	CPutp01-R-	CPutp01-R+	GND-J4	GND
13	Control Plane 2 TPs	UD	GND	GND-J4	CPtp02-DB-	CPtp02-DB+	GND	GND-J4	CPtp02-DA-	CPtp02-DA+
14		GND	CPtp02-DD-	CPtp02-DD+	GND-J4	GND	CPtp02-DC-	CPtp02-DC+	GND-J4	GND
15		UD	GND	GND-J4	CPtp01-DB-	CPtp01-DB+	GND	GND-J4	CPtp01-DA-	CPtp01-DA+
16		GND	CPtp01-DD-	CPtp01-DD+	GND-J4	GND	CPtp01-DC-	CPtp01-DC+	GND-J4	GND

J2, J3, J5-J6 Payload Signal Assignments = User Defined

J1/P1 Switch Slot Signal Assignments

Plug-In Module P1		Row G	Row F	Row E		Row D	Row C	Row B		Row A
				Even	Odd			Even	Odd	
Bplane J1		Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a
1	CPlane Inter-SW UTPs Ports 1 – 4	GDiscrete1	GND	GND-J1	CSutp01-T-	CSutp01-T+	GND	GND-J1	CSutp01-R-	CSutp01-R+
2		GND	CSutp02-T-	CSutp02-T+	GND-J1	GND	CSutp02-R-	CSutp02-R+	GND-J1	GND
3		P1-VBAT	GND	GND-J1	CSutp03-T-	CSutp03-T+	GND	GND-J1	CSutp03-R-	CSutp03-R+
4		GND	CSutp04-T-	CSutp04-T+	GND-J1	GND	CSutp04-R-	CSutp04-R+	GND-J1	GND
5	Control Plane Payload UTPs Ports 1 – 12	SYS_CON*	GND	GND-J1	CPutp01-T-	CPutp01-T+	GND	GND-J1	CPutp01-R-	CPutp01-R+
6		GND	CPutp02-T-	CPutp02-T+	GND-J1	GND	CPutp02-R-	CPutp02-R+	GND-J1	GND
7		Reserved	GND	GND-J1	CPutp03-T-	CPutp03-T+	GND	GND-J1	CPutp03-R-	CPutp03-R+
8		GND	CPutp04-T-	CPutp04-T+	GND-J1	GND	CPutp04-R-	CPutp04-R+	GND-J1	GND
9		UD	GND	GND-J1	CPutp05-T-	CPutp05-T+	GND	GND-J1	CPutp05-R-	CPutp05-R+
10		GND	CPutp06-T-	CPutp06-T+	GND-J1	GND	CPutp06-R-	CPutp06-R+	GND-J1	GND
11		UD	GND	GND-J1	CPutp07-T-	CPutp07-T+	GND	GND-J1	CPutp07-R-	CPutp07-R+
12		GND	CPutp08-T-	CPutp08-T+	GND-J1	GND	CPutp08-R-	CPutp08-R+	GND-J1	GND
13		UD	GND	GND-J1	CPutp09-T-	CPutp09-T+	GND	GND-J1	CPutp09-R-	CPutp09-R+
14		GND	CPutp10-T-	CPutp10-T+	GND-J1	GND	CPutp10-R-	CPutp10-R+	GND-J1	GND
15		Maskable Reset*	GND	GND-J1	CPutp11-T-	CPutp11-T+	GND	GND-J1	CPutp11-R-	CPutp11-R+
16		GND	CPutp12-T-	CPutp12-T+	GND-J1	GND	CPutp12-R-	CPutp12-R+	GND-J1	GND

J2/P2 Switch Slot Signal Assignments

Plug-in Module P2		Row G	Row F	Row E		Row D	Row C	Row B		Row A
				Even	Odd			Even	Odd	
Bplane J2		Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a
1	CPlane Pay UTPs Ports 13 – 16	UD	GND	GND-J2	CPutp13-T-	CPutp13-T+	GND	GND-J2	CPutp13-R-	CPutp13-R+
2		GND	CPutp14-T-	CPutp14-T+	GND-J2	GND	CPutp14-R-	CPutp14-R+	GND-J2	GND
3		UD	GND	GND-J2	CPutp15-T-	CPutp15-T+	GND	GND-J2	CPutp15-R-	CPutp15-R+
4		GND	CPutp16-T-	CPutp16-T+	GND-J2	GND	CPutp16-R-	CPutp16-R+	GND-J2	GND
5	Data Plane Pay-load FP Port 15	UD	GND	GND-J2	DP15-T0-	DP15-T0+	GND	GND-J2	DP15-R0-	DP15-R0+
6		GND	DP15-T1-	DP15-T1+	GND-J2	GND	DP15-R1-	DP15-R1+	GND-J2	GND
7		UD	GND	GND-J2	DP15-T2-	DP15-T2+	GND	GND-J2	DP15-R2-	DP15-R2+
8		GND	DP15-T3-	DP15-T3+	GND-J2	GND	DP15-R3-	DP15-R3+	GND-J2	GND
9	Data Plane Pay-load FP Port 14	UD	GND	GND-J2	DP14-T0-	DP14-T0+	GND	GND-J2	DP14-R0-	DP14-R0+
10		GND	DP14-T1-	DP14-T1+	GND-J2	GND	DP14-R1-	DP14-R1+	GND-J2	GND
11		UD	GND	GND-J2	DP14-T2-	DP14-T2+	GND	GND-J2	DP14-R2-	DP14-R2+
12		GND	DP14-T3-	DP14-T3+	GND-J2	GND	DP14-R3-	DP14-R3+	GND-J2	GND
13	Data Plane Pay-load FP Port 13	UD	GND	GND-J2	DP13-T0-	DP13-T0+	GND	GND-J2	DP13-R0-	DP13-R0+
14		GND	DP13-T1-	DP13-T1+	GND-J2	GND	DP13-R1-	DP13-R1+	GND-J2	GND
15		UD	GND	GND-J2	DP13-T2-	DP13-T2+	GND	GND-J2	DP13-R2-	DP13-R2+
16		GND	DP13-T3-	DP13-T3+	GND-J2	GND	DP13-R3-	DP13-R3+	GND-J2	GND

J3/P3 Switch Slot Signal Assignments

Plug-In Module P3		Row G	Row F	Row E		Row D	Row C	Row B		Row A
				Even	Odd			Even	Odd	
Bplane J3		Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a
1	Data Plane Pay-load FP Port 12	UD	GND	GND-J3	DP12-T0-	DP12-T0+	GND	GND-J3	DP12-R0-	DP12-R0+
2		GND	DP12-T1-	DP12-T1+	GND-J3	GND	DP12-R1-	DP12-R1+	GND-J3	GND
3		UD	GND	GND-J3	DP12-T2-	DP12-T2+	GND	GND-J3	DP12-R2-	DP12-R2+
4		GND	DP12-T3-	DP12-T3+	GND-J3	GND	DP12-R3-	DP12-R3+	GND-J3	GND
5	Data Plane Pay-load FP Port 11	UD	GND	GND-J3	DP11-T0-	DP11-T0+	GND	GND-J3	DP11-R0-	DP11-R0+
6		GND	DP11-T1-	DP11-T1+	GND-J3	GND	DP11-R1-	DP11-R1+	GND-J3	GND
7		UD	GND	GND-J3	DP11-T2-	DP11-T2+	GND	GND-J3	DP11-R2-	DP11-R2+
8		GND	DP11-T3-	DP11-T3+	GND-J3	GND	DP11-R3-	DP11-R3+	GND-J3	GND
9	Data Plane Pay-load FP Port 10	UD	GND	GND-J3	DP10-T0-	DP10-T0+	GND	GND-J3	DP10-R0-	DP10-R0+
10		GND	DP10-T1-	DP10-T1+	GND-J3	GND	DP10-R1-	DP10-R1+	GND-J3	GND
11		UD	GND	GND-J3	DP10-T2-	DP10-T2+	GND	GND-J3	DP10-R2-	DP10-R2+
12		GND	DP10-T3-	DP10-T3+	GND-J3	GND	DP10-R3-	DP10-R3+	GND-J3	GND
13	Data Plane Pay-load FP Port 9	UD	GND	GND-J3	DP09-T0-	DP09-T0+	GND	GND-J3	DP09-R0-	DP09-R0+
14		GND	DP09-T1-	DP09-T1+	GND-J3	GND	DP09-R1-	DP09-R1+	GND-J3	GND
15		UD	GND	GND-J3	DP09-T2-	DP09-T2+	GND	GND-J3	DP09-R2-	DP09-R2+
16		GND	DP09-T3-	DP09-T3+	GND-J3	GND	DP09-R3-	DP09-R3+	GND-J3	GND

J4/P4 Switch Slot Signal Assignments

Plug-in Module P4		Row G	Row F	Row E		Row D	Row C	Row B		Row A
Bplane J4		Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a
1	Data Plane Pay-load FP Port 8	UD	GND	GND-J4	DP08-T0-	DP08-T0+	GND	GND-J4	DP08-R0-	DP08-R0+
2		GND	DP08-T1-	DP08-T1+	GND-J4	GND	DP08-R1-	DP08-R1+	GND-J4	GND
3		UD	GND	GND-J4	DP08-T2-	DP08-T2+	GND	GND-J4	DP08-R2-	DP08-R2+
4		GND	DP08-T3-	DP08-T3+	GND-J4	GND	DP08-R3-	DP08-R3+	GND-J4	GND
5	Data Plane Pay-load FP Port 7	UD	GND	GND-J4	DP07-T0-	DP07-T0+	GND	GND-J4	DP07-R0-	DP07-R0+
6		GND	DP07-T1-	DP07-T1+	GND-J4	GND	DP07-R1-	DP07-R1+	GND-J4	GND
7		UD	GND	GND-J4	DP07-T2-	DP07-T2+	GND	GND-J4	DP07-R2-	DP07-R2+
8		GND	DP07-T3-	DP07-T3+	GND-J4	GND	DP07-R3-	DP07-R3+	GND-J4	GND
9	Data Plane Pay-load FP Port 6	UD	GND	GND-J4	DP06-T0-	DP06-T0+	GND	GND-J4	DP06-R0-	DP06-R0+
10		GND	DP06-T1-	DP06-T1+	GND-J4	GND	DP06-R1-	DP06-R1+	GND-J4	GND
11		UD	GND	GND-J4	DP06-T2-	DP06-T2+	GND	GND-J4	DP06-R2-	DP06-R2+
12		GND	DP06-T3-	DP06-T3+	GND-J4	GND	DP06-R3-	DP06-R3+	GND-J4	GND
13	Data Plane Pay-load FP Port 5	UD	GND	GND-J4	DP05-T0-	DP05-T0+	GND	GND-J4	DP05-R0-	DP05-R0+
14		GND	DP05-T1-	DP05-T1+	GND-J4	GND	DP05-R1-	DP05-R1+	GND-J4	GND
15		UD	GND	GND-J4	DP05-T2-	DP05-T2+	GND	GND-J4	DP05-R2-	DP05-R2+
16		GND	DP05-T3-	DP05-T3+	GND-J4	GND	DP05-R3-	DP05-R3+	GND-J4	GND

J5/P5 Switch Slot Signal Assignments

Plug-in Module P5		Row G	Row F	Row E		Row D	Row C	Row B		Row A
Bplane J5		Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a
1	Data Plane Pay-load FP Port 4	UD	GND	GND-J5	DP04-T0-	DP04-T0+	GND	GND-J5	DP04-R0-	DP04-R0+
2		GND	DP04-T1-	DP04-T1+	GND-J5	GND	DP04-R1-	DP04-R1+	GND-J5	GND
3		UD	GND	GND-J5	DP04-T2-	DP04-T2+	GND	GND-J5	DP04-R2-	DP04-R2+
4		GND	DP04-T3-	DP04-T3+	GND-J5	GND	DP04-R3-	DP04-R3+	GND-J5	GND
5	Data Plane Pay-load FP Port 3	UD	GND	GND-J5	DP03-T0-	DP03-T0+	GND	GND-J5	DP03-R0-	DP03-R0+
6		GND	DP03-T1-	DP03-T1+	GND-J5	GND	DP03-R1-	DP03-R1+	GND-J5	GND
7		UD	GND	GND-J5	DP03-T2-	DP03-T2+	GND	GND-J5	DP03-R2-	DP03-R2+
8		GND	DP03-T3-	DP03-T3+	GND-J5	GND	DP03-R3-	DP03-R3+	GND-J5	GND
9	Data Plane Pay-load FP Port 2	UD	GND	GND-J5	DP02-T0-	DP02-T0+	GND	GND-J5	DP02-R0-	DP02-R0+
10		GND	DP02-T1-	DP02-T1+	GND-J5	GND	DP02-R1-	DP02-R1+	GND-J5	GND
11		UD	GND	GND-J5	DP02-T2-	DP02-T2+	GND	GND-J5	DP02-R2-	DP02-R2+
12		GND	DP02-T3-	DP02-T3+	GND-J5	GND	DP02-R3-	DP02-R3+	GND-J5	GND
13	Data Plane Pay-load FP Port 1	UD	GND	GND-J5	DP01-T0-	DP01-T0+	GND	GND-J5	DP01-R0-	DP01-R0+
14		GND	DP01-T1-	DP01-T1+	GND-J5	GND	DP01-R1-	DP01-R1+	GND-J5	GND
15		UD	GND	GND-J5	DP01-T2-	DP01-T2+	GND	GND-J5	DP01-R2-	DP01-R2+
16		GND	DP01-T3-	DP01-T3+	GND-J5	GND	DP01-R3-	DP01-R3+	GND-J5	GND

J6/P6 Switch Slot Signal Assignments

Plug-In Module P6		Row G	Row F	Row E		Row D	Row C	Row B		Row A
				Even	Odd			Even	Odd	
Bplane J6		Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a
1	Data Plane Inter-SW FP Port 4	UD	GND	GND-J6	DS04-T0-	DS04-T0+	GND	GND-J6	DS04-R0-	DS04-R0+
2		GND	DS04-T1-	DS04-T1+	GND-J6	GND	DS04-R1-	DS04-R1+	GND-J6	GND
3		UD	GND	GND-J6	DS04-T2-	DS04-T2+	GND	GND-J6	DS04-R2-	DS04-R2+
4		GND	DS04-T3-	DS04-T3+	GND-J6	GND	DS04-R3-	DS04-R3+	GND-J6	GND
5	Data Plane Inter-SW FP Port 3	UD	GND	GND-J6	DS03-T0-	DS03-T0+	GND	GND-J6	DS03-R0-	DS03-R0+
6		GND	DS03-T1-	DS03-T1+	GND-J6	GND	DS03-R1-	DS03-R1+	GND-J6	GND
7		UD	GND	GND-J6	DS03-T2-	DS03-T2+	GND	GND-J6	DS03-R2-	DS03-R2+
8		GND	DS03-T3-	DS03-T3+	GND-J6	GND	DS03-R3-	DS03-R3+	GND-J6	GND
9	Data Plane Inter-SW FP Port 2	UD	GND	GND-J6	DS02-T0-	DS02-T0+	GND	GND-J6	DS02-R0-	DS02-R0+
10		GND	DS02-T1-	DS02-T1+	GND-J6	GND	DS02-R1-	DS02-R1+	GND-J6	GND
11		UD	GND	GND-J6	DS02-T2-	DS02-T2+	GND	GND-J6	DS02-R2-	DS02-R2+
12		GND	DS02-T3-	DS02-T3+	GND-J6	GND	DS02-R3-	DS02-R3+	GND-J6	GND
13	Data Plane Inter-SW FP Port 1	UD	GND	GND-J6	DS01-T0-	DS01-T0+	GND	GND-J6	DS01-R0-	DS01-R0+
14		GND	DS01-T1-	DS01-T1+	GND-J6	GND	DS01-R1-	DS01-R1+	GND-J6	GND
15		UD	GND	GND-J6	DS01-T2-	DS01-T2+	GND	GND-J6	DS01-R2-	DS01-R2+
16		GND	DS01-T3-	DS01-T3+	GND-J6	GND	DS01-R3-	DS01-R3+	GND-J6	GND

6U, 17-Slot Signal Assignments

J0 Signal Assignments

	Row I	Row H	Row G	Row F	Row E	Row D	Row C	Row B	Row A
1	Vs1	Vs1	Vs1	Vs1	No Pad	Vs2	Vs2	Vs2	Vs2
2	Vs1	Vs1	Vs1	Vs1	No Pad	Vs2	Vs2	Vs2	Vs2
3	Vs3	Vs3	Vs3	Vs3	No Pad	Vs3	Vs3	Vs3	Vs3
4	GND	SM2	SM3	GND	-12V_Aux	GND	SYSRESET*	NVMRO	GND
5	GND	GAP*	GA4*	GND	3.3V_Aux	GND	SM0	SM1	GND
6	GND	GA3*	GA2*	GND	+12V_Aux	GND	GA1*	GA0*	GND
7	TCK	GND	GND	TDO	TDI	GND	GND	TMS	TRST*
8	GND	REF_CLK-	REF_CLK+	GND	GND	AUX_CLK-	AUX_CLK+	GND	GND

J2/P2 - J6/P6 Signal Assignments**

Plug in Module P2–P6				Row G	Row F	Row E Even	Row E Odd	Row D	Row C	Row B Even	Row B Odd	Row A
Backplane J2–J6				Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a
1	X16 using [15:0]	x8 using [7:0]	x4 using [3:0]	SEwafer1	GND	GND-J2	LN0-TD-	LN0-TD+	GND	GND-J2	LN0-RD-	LN0-RD+
2				GND	LN1-TD-	LN1-TD+	GND-J2	GND	LN1-RD-	LN1-RD+	GND-J2	GND
3				SEwafer3	GND	GND-J2	LN2-TD-	LN2-TD+	GND	GND-J2	LN2-RD-	LN2-RD+
4				GND	LN3-TD-	LN3-TD+	GND-J2	GND	LN3-RD-	LN3-RD+	GND-J2	GND
5			x4 using [7:4]	SEwafer5	GND	GND-J2	LN4-TD-	LN4-TD+	GND	GND-J2	LN4-RD-	LN4-RD+
6				GND	LN5-TD-	LN5-TD+	GND-J2	GND	LN5-RD-	LN5-RD+	GND-J2	GND
7				SEwafer7	GND	GND-J2	LN6-TD-	LN6-TD+	GND	GND-J2	LN6-RD-	LN6-RD+
8				GND	LN7-TD-	LN7-TD+	GND-J2	GND	LN7-RD-	LN7-RD+	GND-J2	GND
9		x8 using [15:8]	x4 using [11:8]	SEwafer9	GND	GND-J2	LN8-TD-	LN8-TD+	GND	GND-J2	LN8-RD-	LN8-RD+
10				GND	LN9-TD-	LN9-TD+	GND-J2	GND	LN9-RD-	LN9-RD+	GND-J2	GND
11				SEwafer11	GND	GND-J2	LN10-TD-	LN10-TD+	GND	GND-J2	LN10-RD-	LN10-RD+
12				GND	LN11-TD-	LN11-TD+	GND-J2	GND	LN11-RD-	LN11-RD+	GND-J2	GND
13			x4 using [15:12]	SEwafer13	GND	GND-J2	LN12-TD-	LN12-TD+	GND	GND-J2	LN12-RD-	LN12-RD+
14				GND	LN13-TD-	LN13-TD+	GND-J2	GND	LN13-RD-	LN13-RD+	GND-J2	GND
15				SEwafer15	GND	GND-J2	LN14-TD-	LN14-TD+	GND	GND-J2	LN14-RD-	LN14-RD+
16				GND	LN15-TD-	LN15-TD+	GND-J2	GND	LN15-RD-	LN15-RD+	GND-J2	GND

**Any signal pins pass through the rear

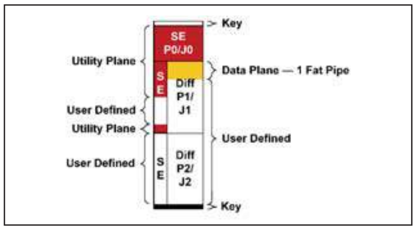
J1/P1 Signal Assignments Slots 4-15

Plug-In Module P1		Row G	Row F	Row E Even	Row E Odd	Row D	Row C	Row B Even	Row B Odd	Row A
Bplane J1		Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a
1	Data Plane Port 1	GDiscrete1	GND	GND-J1	DP01-T0-	DP01-T0+	GND	GND-J1	DP01-R0-	DP01-R0+
2		GND	DP01-T1-	DP01-T1+	GND-J1	GND	DP01-R1-	DP01-R1+	GND-J1	GND
3		P1-VBAT	GND	GND-J1	DP01-T2-	DP01-T2+	GND	GND-J1	DP01-R2-	DP01-R2+
4		GND	DP01-T3-	DP01-T3+	GND-J1	GND	DP01-R3-	DP01-R3+	GND-J1	GND
5	Data Plane Port 2	SYS_CON*	GND	GND-J1	DP02-T0-	DP02-T0+	GND	GND-J1	DP02-R0-	DP02-R0+
6		GND	DP02-T1-	DP02-T1+	GND-J1	GND	DP02-R1-	DP02-R1+	GND-J1	GND
7		Reserved	GND	GND-J1	DP02-T2-	DP02-T2+	GND	GND-J1	DP02-R2-	DP02-R2+
8		GND	DP02-T3-	DP02-T3+	GND-J1	GND	DP02-R3-	DP02-R3+	GND-J1	GND
9	Data Plane Port 3	UD	GND	GND-J1	DP03-T0-	DP03-T0+	GND	GND-J1	DP03-R0-	DP03-R0+
10		GND	DP03-T1-	DP03-T1+	GND-J1	GND	DP03-R1-	DP03-R1+	GND-J1	GND
11		UD	GND	GND-J1	DP03-T2-	DP03-T2+	GND	GND-J1	DP03-R2-	DP03-R2+
12		GND	DP03-T3-	DP03-T3+	GND-J1	GND	DP03-R3-	DP03-R3+	GND-J1	GND
13	Data Plane Port 4	UD	GND	GND-J1	DP04-T0-	DP04-T0+	GND	GND-J1	DP04-R0-	DP04-R0+
14		GND	DP04-T1-	DP04-T1+	GND-J1	GND	DP04-R1-	DP04-R1+	GND-J1	GND
15		Maskable Reset*	GND	GND-J1	DP04-T2-	DP04-T2+	GND	GND-J1	DP04-R2-	DP04-R2+
16		GND	DP04-T3-	DP04-T3+	GND-J1	GND	DP04-R3-	DP04-R3+	GND-J1	GND

*Slots 16 and 17 = User Defined

3U, 3-Slot Peripheral Profile

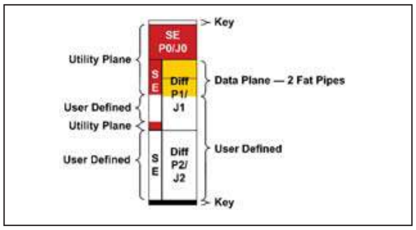
BKP3-CEN03-15.2.9



SLT3-PER-1F-14.3.2

3U, 3-Slot Paylod Profile

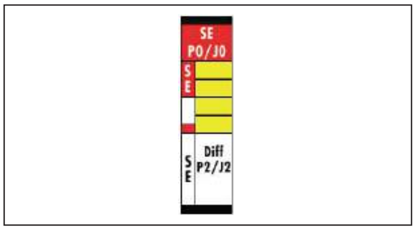
BKP3-CEN03-15.2.9



SLT3-PAY-2F-14.2.7

3U, 5-Slot Switch Profile (Slots 1-2)

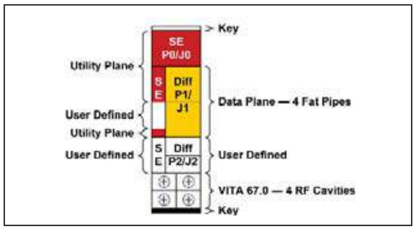
BKP3-DIS05-15.3.2



SLT3-SWH-4F-14.4.4

3U, 5-Slot Paylod Profile (Slots 3-5)

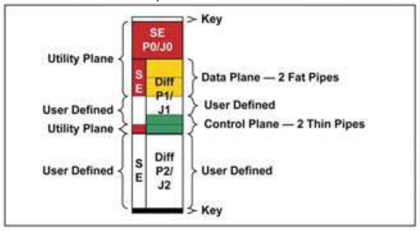
BKP3-DIS05-15.3.2



SLT3-PAY-4F4R-14.6.2

3U, 6-Slot Payload Profile

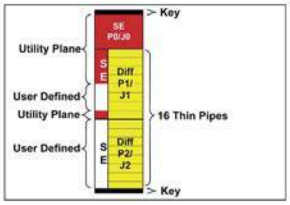
BKP3-DIS06-15.2.14, BKP3-DIS06-15.2.7



SLT3-PAY-2F2T-14.2.5

3U, 6-Slot Switch Profile

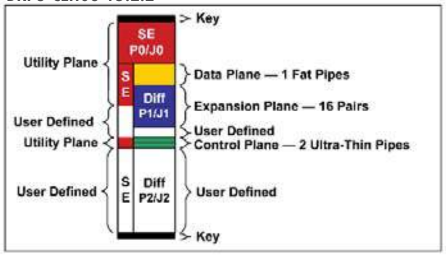
BKP3-DIS06-15.2.14, BKP3-DIS06-15.2.7



SLT3-SWH-16T-14.4.6

3U, 6-Slot Payload Profile

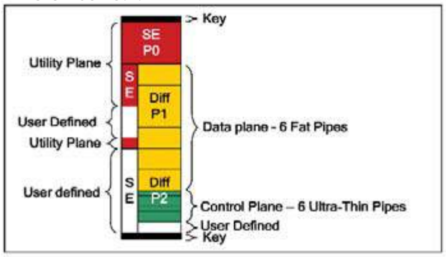
BKP3-CEN06-15.2.2



SLT3-PAY-1F2F2U-14.2.2

3U, 6-Slot Switch Profile

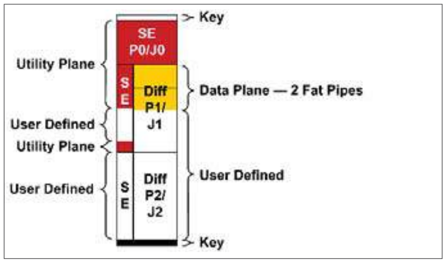
BKP3-CEN06-15.2.2



SLT3-SWH-6F6U-14.4.1

3U, 6-Slot Payload Profile

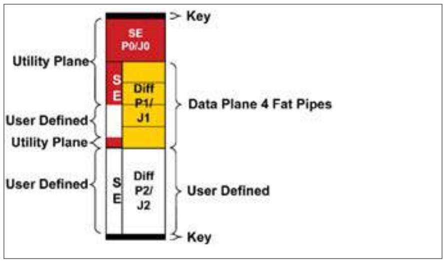
BKP3-CEN06-15.2.12



SLT3-PAY-2F-14.2.7

3U, 6-Slot Switch Profile

BKP3-CEN06-15.2.12

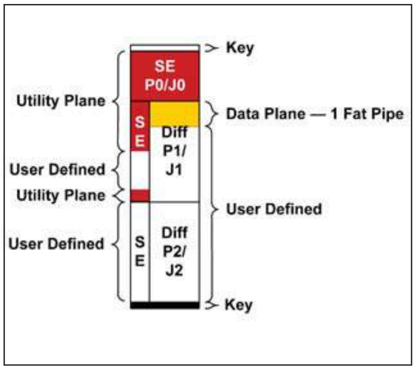


SLT3-SWH-4F-14.4.4

OpenVPX Backplanes - Slot Profiles

3U, 6-Slot Peripheral Profile

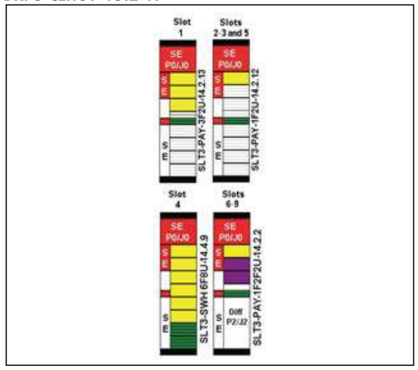
BKP3-CEN06-15.2.12



SLT3-PER-1F-14.3.2

3U, 9-Slot Profiles

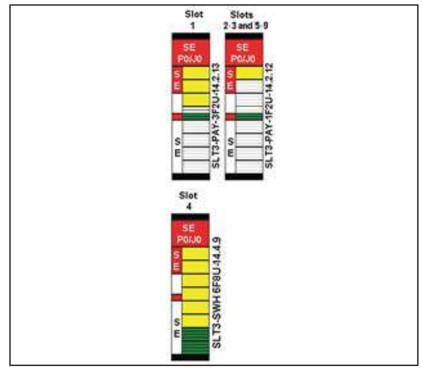
BKP3-CEN09-15.2-17



BKP3-CEN09-15.2-17-1 with switch in slot 4 with expansion plane

3U, 9-Slot Profiles

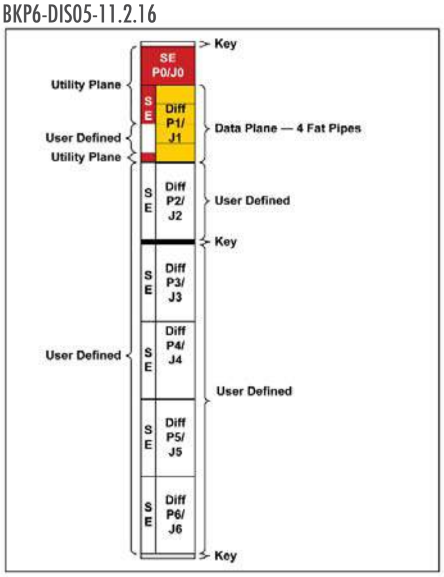
BKP3-CEN09-15.2-17



BKP3-CEN09-15.2-17-3 with switch in slot 4 without expansion plane

6U, 5-Slot Payload Profile

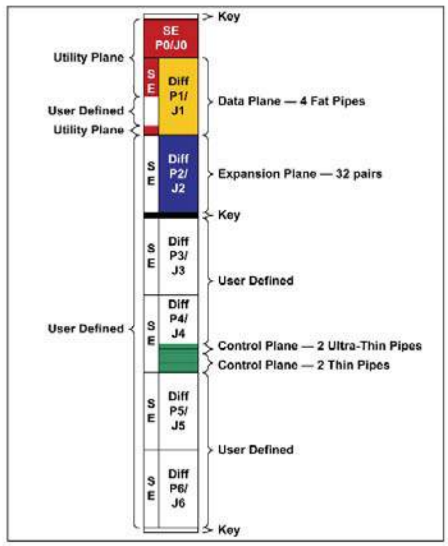
BKP6-DIS05-11.2.16



SLT6-PER-4F-10.3.1

6U, 5-Slot Payload Profile

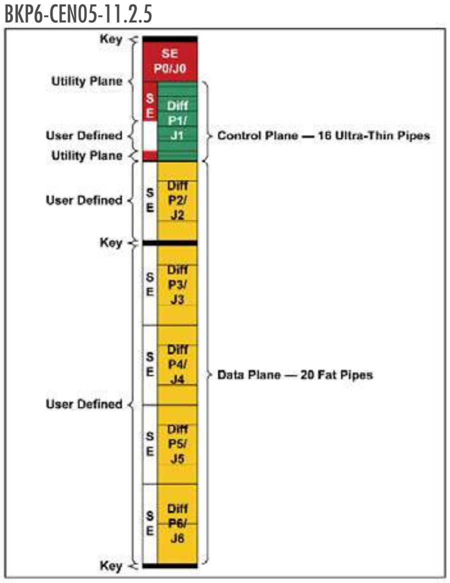
BKP6-CEN05-11.2.5



SLT6-PAY-4F1Q2U2T-10.2.1

6U, 5-Slot Switch Profile

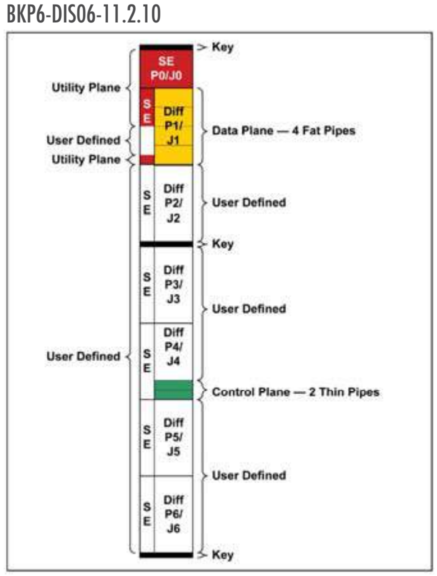
BKP6-CEN05-11.2.5



SLT6-SWH-16U20F-10.4.2

6U, 6-Slot Payload Profile

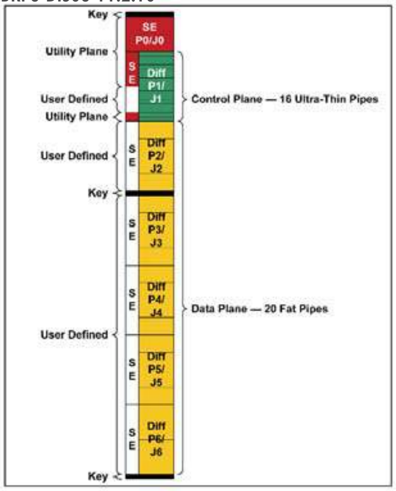
BKP6-DIS06-11.2.10



SLT6-PAY-4F2T-10.2.2

6U, 6-Slot Switch Profile

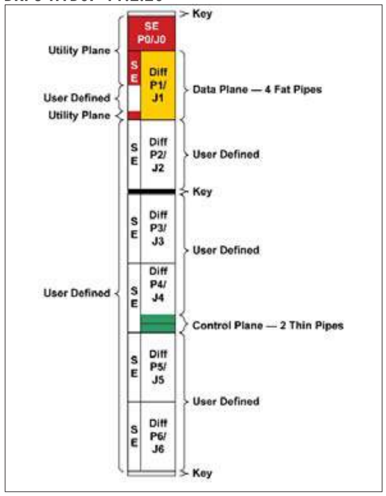
BKP6-DIS06-11.2.10



SLT6-SWH-4F24T-10.4.4

6U, 7-Slot Peripheral Profile

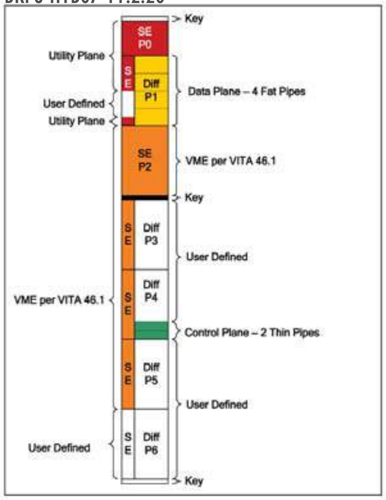
BKP6-HYB07-11.2.20



SLT6-PAY-4F2T-10.2.2

6U, 7-Slot Bridge Profile

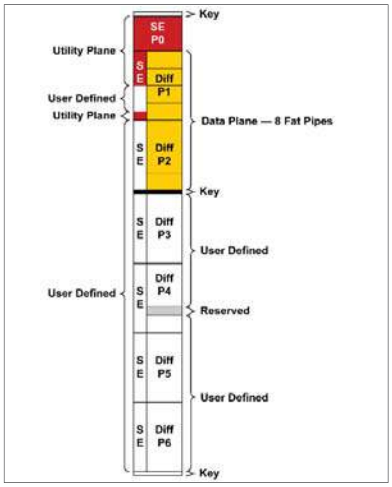
BKP6-HYB07-11.2.20



SLT6-BRG-4F1V2T-10.5.1

6U, 9-Slot Payload Profile

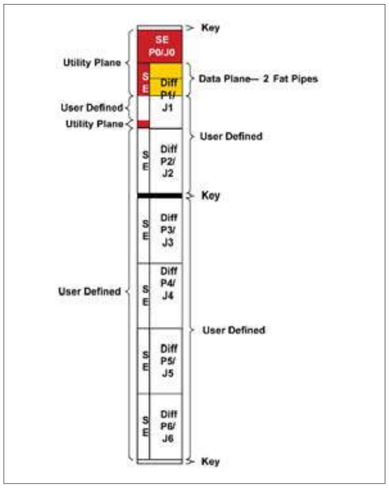
BKP6-CEN09-11.2.13



SLT6-PAY-8F-10.2.3

6U, 9-Slot Peripheral Profile

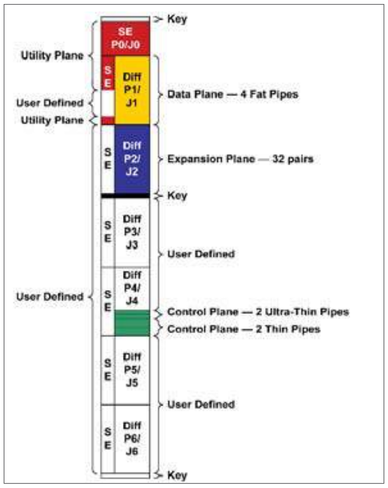
BKP6-CEN09-11.2.13



SLT6-PER-2F-10.3.2

6U, 10-Slot Payload Profile

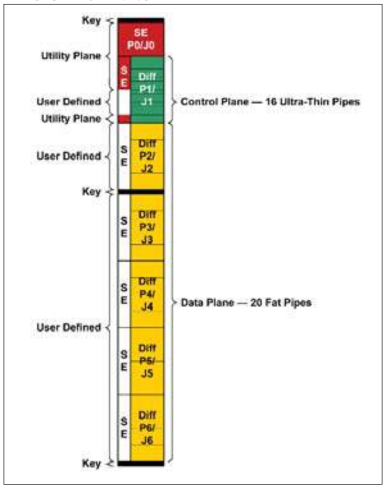
BKP6-CEN10-11.2.6



SLT6-PAY-4F1Q2U2T-10.2.1

6U, 10-Slot Switch Profile

BKP6-CEN10-11.2.6

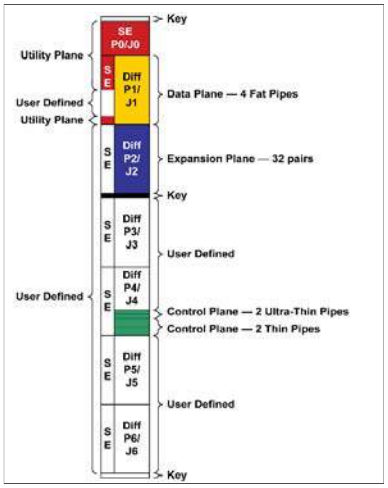


SLT6-SWH-16U20F-10.4.2

OpenVPX Backplanes - Slot Profiles

6U, 16-Slot Payload Profile

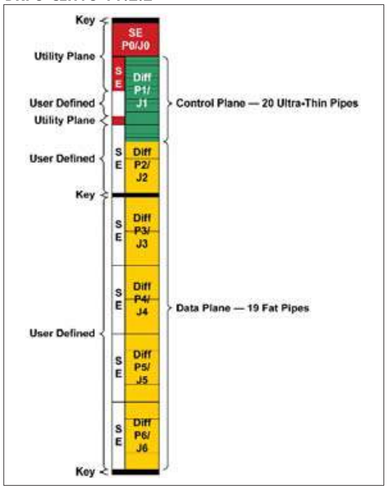
BKP6-CEN16-11.2.2



SLT6-PAY-4F1Q2U2T-10.2.1

6U, 16-Slot Switch Profile

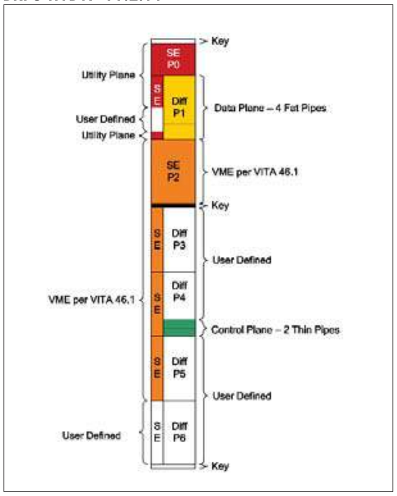
BKP6-CEN16-11.2.2



SLT6-SWH-20U19F-10.4.1

6U, 17-Slot VME Profile

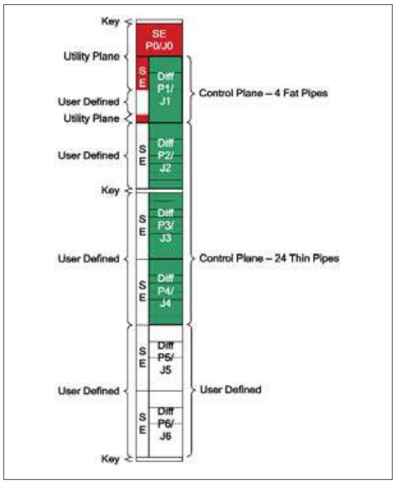
BKP6-HYB17-11.2.11



SLT6-BRG-4F1V2T-10.5.1

6U, 17-Slot Switch Profile

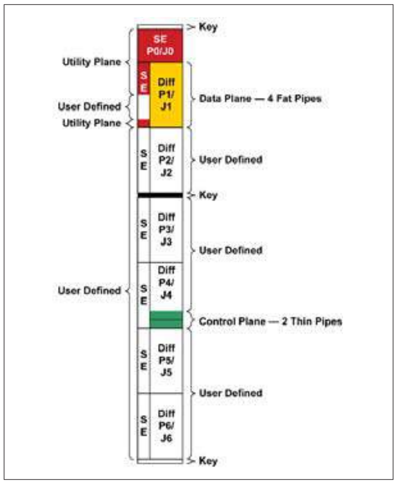
BKP6-HYB17-11.2.11



SLT6-SWH-4F24T-10.4.4

6U, 17-Slot Payload Profile

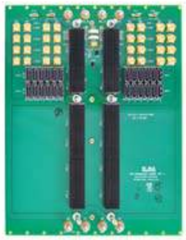
BKP6-HYB17-11.2.11



SLT6-PAY-4F2T-10.2.2

VPX Test Backplane

Version without SMA/SATA



Version with SMA/SATA

Features

- For convenient testing of VPX/OpenVPX boards
- Designed to meet the latest VITA 46.0 and VITA 65 specifications
- Accepts either 3U or 6U VPX cards by use of the configuration jumpers on the rear of the backplane and a 3U shelf divider
- Wider slot pitch allows more space for attaching to probes SMA/SATA version has J1 "A" channel broken out to sixteen SMA connectors for each slot (32 total)
- SMA/SATA version has J1 "B", "C", and "D" channels are each broken out to four SATA II cable headers for a total of 12 headers per slot (24 total)
- Allows simultaneous access of J1 fabric signals with standard VPX RTM module for J2-J6 signals
- More than two VPX modules may be interconnected by using additional 2-slot test backplanes

Mechanical Specifications

Version	Height	Slots
for direct wafer to wafer MultiGig cable connection	6U	2
with SMA/SATA	6U	2

Multi-Gig RT-2 connectors

Board Specifications

Version	Slots	Layers	2 oz. Copper Power & Ground	PCB FR-4 or Equivalent	PCB Thickness
for direct wafer to wafer MultiGig cable connection	2	10	Yes	Yes	.213"
with SMA/SATA	2	8	Yes	Yes	.213"

The Elma Bustronic 2-slot test backplanes are unique tools that lets VPX card developers and system integrators test VPX boards. The device allows the user to power up test their J1 fabric connections as they would be interconnected in the target application. Signals can be passed from one slot to the next via high speed interconnecting cables or via signals introduced through the J1 fabric connector. The SMA/SATA version also allows access for these types of connections. Additional 2-slot Test Backplanes can be used in a larger chassis to interconnect the J1 primary fabric in any serial topology desired. Signals in any other connector position may be interconnected or accessed using optional MultiGig cable headers or typical commercial RTM modules. Note that rear cables and RTM connectors cannot be used at the same time in the same slot.

Unlike other access methods, such as rear VPX cables alone or special high speed RTM break out boards, the Elma Bustronic 2-slot Test backplane allows primary J1 fabric signals to be accessed/interconnected/injected without interfering with the use of an existing RTM module designed for J2-J6 IO connector signals. Custom backplanes are often required to interconnect the primary fabric signals between multiple VPX blades for a specific application. However, it is desirable to be able to connect two or more such blades with a test backplane before investing the time or expense of a custom VPX backplane.

Order Information

Version	Height	Slots	Order Number
For direct wafer to wafer MultiGig cable connection	6U	2	1900002311-0000
With SMA/SATA	6U	2	1900002083-0000

Features

- Compliant to latest VITA 46 specifications
- Power and ground only for VPX development purposes
- 3.3V, 5V, and 12V power
- Simple and low-cost development backplane
- P0-P6 pins are user-defined

Mechanical Specifications

Height	Slots
3U	1, 5, 6
7U	1, 4

Multi-Gig RT-2 connectors

Board Specifications

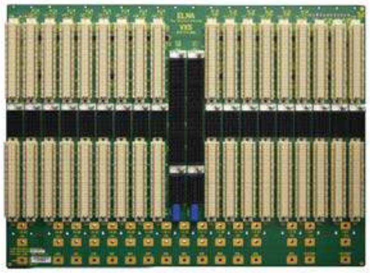
Version	Layers	2 oz. Copper Power & Ground	PCB UL Recognized 94V-0	PCB FR-4 or Equivalent	PCB Thickness
3U	10	Yes	Yes	Yes	.212”
7U	10	Yes	Yes	Yes	.212”

The VPX power and ground development backplane is a simple and cost-effective development tool. All of the pins are user defined. Power for 3.3V, 5V and 12V are included. The rear connectors are all fully loaded.

Order Information

Height	Slots	Description	Order Number
3U	1	1-slot VPX power and ground	101VPX301P-1X31R
3U	5	5-slot VPX power and ground	101VPX305P-1X31R
3U	6	6-slot VPX power and ground	101VPX306P-1X31R
7U	1	1-slot VPX power and ground	101VPX701P-1X40R
7U	1	1-slot VPX power & ground w/VITA 67 RF	1900002558-0000
7U	4	4-slot VPX power and ground	101VPX704P-1X40R*

* Consult factory for ordering details



The VITA 41.0 specification for VXS was ratified by ANSI in 2006. VXS adds a high-speed connector over P0 of a VME64x backplane for serial data traffic. Designers have the flexibility of plugging in standard VME64x cards for parallel bus only, integrate new payload and switch cards for parallel bus and switch fabric transport or switch fabric transport only. The VXS spec allows for four differential serial pairs per direction link over P0, and supports up to two such ports on each VMEbus card.

Backwards Compatibility

One important consideration for VME as it has evolved over the years is its backwards compatibility. From three row 16 bit, 40 Mbytes/sec to 32- bit (3U) and 64-bit (6U) (80 Mbytes/sec) to five row VME64x (160Mbytes/sec), VME has always had increased performance along with compatibility to previous specifications. VXS is no exception. The VXS design starts with a standard VME64x backplane design and implements a high speed fabric by replacing the existing P0 connector with the Multi-Gig 7 Row connector and adding hub slots fully populated with the new connector. However, the backplane is backwards compatible to VME64x/VME, allowing standard VME and VME64x cards (without the P0 connector) to be used in the system.

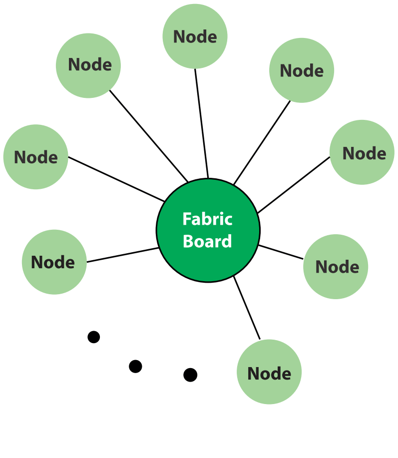
Backwards compatibility is a highly important issue. Here are some of the key reasons to maintain it:

- Preservation of investment in a technology
- Reuse of existing cards/components with ability to upgrade
- Working on a proven, tested platform
- Multiple vendors/choices of legacy platform
- Less risk of obsolescence - as new compatible products are available in roadmap.

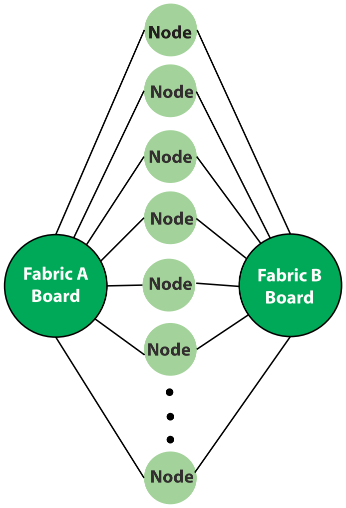
Signal Integrity

At higher clock speeds, the PCB requires cleaner signal transmission without compromising the stability of the system. Signal integrity issues such as reflections, cross talk, frequency dependent transmission line loss and dispersion can significantly lead to poorer system performance propagating through the interconnect.

Depending on the configuration, routing a VXS backplane with superior performance can be challenging. In the higher slot sizes, the number and length of the traces can have an effect on the signal integrity. Particularly with larger backplane the number of traces and lack of physical space, it may require creative and intelligent routing schemes from an experienced designer.



Star - One Fabric

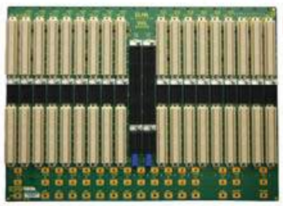


Dual Star - Two Fabric Slots

VXS Backplanes - Star, Dual Star, Switchless Mesh

Star

Switchless Mesh



Dual Star

Features

- Conforms to VITA 41.0-2006 VXS backplane specifications
- Versions compliant to VITA 41.6 for Ethernet Control Plane are available
- High speed MultiGig RT-2 connector over P0
- One hub slot, 4 payload slots (5-slot)
- One switch slot, 7 payload slots, and 2 legacy VME64x slots (10-slot)
- Plenty of power bugs for 3.3V, 5V, 12V and GND
- Compatible with VME64x standard line cards
- Single Star, Dual Star, Mesh, and Hybrid versions available
- Various configurations of payload slots, switch card slots, etc.

Mechanical Specifications

Version	Slots	Height
Star	5, 8 and 10 slots, other sizes available	7U height (5-slot) , 6U height (8, 10-slot)
Dual Star	8, 12, 18, and 20 slots, other sizes available	6U (8, 18, 21-slot), 7U (12, 20-slot)
Switchless Mesh	5 slots, other sizes available	7U

160-pin, class II VME connectors
Multi-Gig RT-2 connectors

Board Specifications

Version	Layers	2 oz. Copper Power & Ground	PCB UL Recognized 94V-0	PCB FR-4 or Equivalent	PCB Thickness
Star	12, 14-layers	Yes	Yes	Yes	PCB .159” thick (5-slot) PCB .182” thick (8-slot) PCB .145” thick (10-slot)
Dual Star	10-layer (8-slot), 12-layer (12-slot Nelco), 18-layer (18-slot Nelco, 20, Nelco)	Yes	Yes	Yes	PCB .147” thick (8-slot) PCB .160” thick (12- slot) PCB .198” thick (12-slot Nelco) PCB .157” thick (18, 20, 21-slot)
Switchless Mesh	10 layers	Yes	Yes	Yes	PCB .148” thick

Order Information

101VXS □□□□ - □□□□□

□ Height

6 = 6U
7 = 7U

□ Topology

S = Single Star
D = Dual Star
M = Switchless Mesh
T = Single Star w/ VITA 41.6 Control Plane
M = Dual Star w/ VITA 41.6 Control Plane

□□ Slots

02-14

□ Power Interface

0 = 10 pin power tap with 6/32 screw
1 = M4 threaded stud
2 = 10 pin power taps with busbar kit
9 = Custom
X = Not applicable

□ J1 Connectors and Shrouds

0 = Not applicable
1 = Not applicable
2 = 160 pin 17mm with shrouds, all slots
3 = 160 pin 13mm with shrouds, all slots
4 = 160 pin 13mm without shrouds, all slots
5 = 160 pin 17mm without shrouds, all slots
6 = 160 pin 5mm without shrouds, all slots
7 = 160 pin 17mm slot 1, 5mm all slots
X = Not applicable

□ J2 Connectors and Shrouds

0 = Not applicable
1 = Not applicable
2 = 160 pin 17mm with shrouds, all slots
3 = 160 pin 13mm with shrouds, all slots
4 = 160 pin 13mm without shrouds, all slots
5 = 160 pin 17mm without shrouds, all slots
6 = 160 pin 5mm without shrouds, all slots
X = Not applicable

□ J0 Connectors and Shrouds

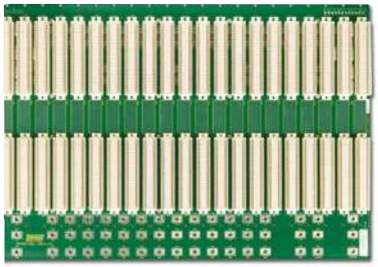
0 = No J0 connector
1 = J0 (9 x 15 connector)
2 = J0, RJ0, rear alignment pin and header (if VME64x slots present, J0 and shrouds inst.)
X = Not applicable

□□□□

Common Order Number Suffixes For Power & Shrouds

-0621 -0621R

If an R is present at the end of the order#, the backplane is RoHS compliant.



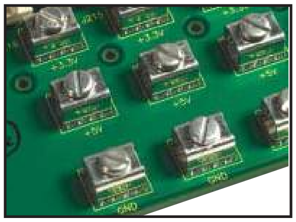
The Elma Bustronic VME64x backplane series is designed to fully comply with the ANSI/VITA VME extension standard. We provide all standard features required for VME64x compatibility, including 160-pin VME extension connectors in J1 and J2, all defined ground pins connected to a ground plane, routing and termination of all VME and VME64x bussed signal lines, geographic address pins, distribution of +5V, +3.3V, +/-12V, +/-V1, +/-V2, and VPC, all on a single monolithic printed circuit board with J1 and J2 included. Additional features include active, electronic IACK/BUSGRANT daisy chaining standard; onboard, inboard termination; distributed high frequency capacitors for each slot, distributed low frequency capacitors; five signal layers, five power and ground planes.

Elma Bustronic constructs the VME64x board in ten layers — five signal layers, five power and ground planes. We incorporate a full stripline design, generously distributed decoupling capacitors, inboard termination, and 2 oz. power and ground planes. We could use fewer layers, but we use this design to isolate each signal layer so our backplanes provide superior performance. Our VME64x backplanes are compliant to the VITA 1.7 Increased Current Specification.

Power Distribution

The Elma Bustronic 7U VME64x backplane families are designed with the power insertion area below the signal slots above the bottom-mounting rail so we can apply the maximum power potential to the backplane. We have inserted adequate numbers of power bugs in this area to accommodate more power than the 12 amps potential per slot. The 6U VME64X and VME320 backplanes have power bugs on top and below the slots. As an option, we offer 8/32" press-in powerstuds. +/- V1 and V2 are accommodated by a 12-pin friction lock header connector located at the top of the backplane and an 8-position utility connector for system functions, including Ground, +5V, ACFAIL, SYSFAIL, SYSRESET, +3.3V, +12V, and -12V.

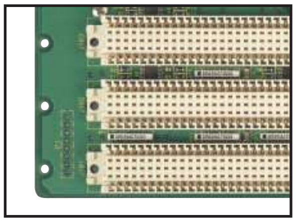
Power Bug



Signal Layout

The Elma Bustronic design conforms to ANSI/VITA 1.1-1997 (R2003). Onboard, inboard terminators are provided to reduce signal length and reduce possible signal reflections. A minimum stub length is utilized in routing and interconnecting to the terminators. IACK/BUSGRANT daisy chaining is accomplished utilizing surface mount components located between the J1 connectors. Elma Bustronic designs backplanes with the customer's system design in mind to ensure the highest performance, reliability, and value.

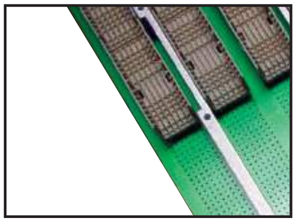
Optional - Busbar



Automatic Daisy Chaining

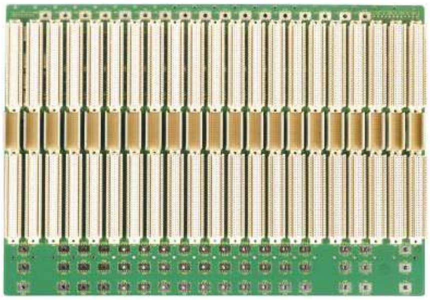
Automatic daisy chain in VME64x backplanes eliminates a major source of problems when configuring a VME64x system, while eliminating the need for access to the backplane. The VME64x backplane uses surface mount ICs for the daisy chaining. SMT is the latest in technology and offers the most space-saving and efficient processes. The VME320 backplanes have manual jumpering.

Optional - Stiffeners



For more information see VME Reference Sheet at
http://www.elmabustronic.com/CatalogInfo

VME64x Backplanes - 6U, 7U



Features

- Meets or exceeds ANSI/VITA 1.1-1997 (R2003), VME extensions standard
- Exceeds ANSI/VITA 1-1994 (R2002) and IEEE 1014-1987 specifications
- 10-layer controlled impedance stripline design
- Active BUSGRANT, IACK daisy chain
- 7U versions have extra power bugs at bottom of backplane
- Superior power distribution
- Backplane stiffeners to provide durability, reliability
- Versions compliant to VITA 1.7 Increased Current Specification
- Optional conformal coating for rugged applications

Mechanical Specifications

Height	Slots
6U*	5, 8, 12, 14, 15 & 21 (other sizes available)
7U*	2-21
Vibration: to DIN 41640 Part 15:10 Hz-500Hz 5 g rms, Impact (10 impacts per axis x. y. z) 100 g, 6 ms	

*160-pin, class II VME connectors

Board Specifications

Type	Layers	2 oz. Copper Power & Ground	PCB UL Recognized 94V-0	PCB FR-4 or Equivalent	PCB Thickness
6U	10	Yes	Yes	Yes	.125”
7U	10	Yes	Yes	Yes	.125”

Electrical/Operating

Operating Temperature:
–40˚C to +85˚C
Storage Temperature:
–55˚C to 85˚C
Single Line Impedance:
55 Ohm +/- 10 %. Resistance
Basic Current Consumption:
1.5A Max. voltage drop for +5V and +3.3V< 40mV (at 9A/slot)

Order Information

101V64X ☐☐☐ - ☐☐☐☐

☐ Form

M = Monolithic, J1/J2, 7U
C = Monolithic, J1/J2, 6U

☐☐ Slots

02-21 (7U)
05, 08, 12*, 14, 15 & 21* slots (6U, other sizes available)

☐ Power Interface

0 = 10 pin power tap with 6/32 screw
1 = M4 threaded stud
2 = 10 pin power taps with busbar kit
8 = Not applicable
9 = Custom (-9XXX sequential Numbers)

☐ J1 Connectors and Shrouds

0 = 96 pin, 13mm with shrouds first and last slots, all other slots 96 pin, 6mm connectors
1 = 96 pin, 17mm with shrouds first and last slots, all other slots 96 pin, 6mm connectors
2 = 160 pin, 17mm with shrouds, all slots
3 = 160 pin, 13mm with shrouds, all slots
4 = 160 pin, 13mm without shrouds, all slots
5 = 160 pin, 17mm without shrouds, all slots
6 = 160 pin, 5mm without shrouds, all slots

☐ J2 Connectors and Shrouds

0 = 96 pin, 13mm with shrouds
1 = 96 pin, 17mm with shrouds
2 = 160 pin, 13mm with shrouds, all slots
3 = 160 pin, 13mm with shrouds, all slots
4 = 160 pin, 13mm without shrouds, all slots
5 = 160 pin, 17mm without shrouds, all slots
6 = 160 pin, 5mm without shrouds, all slots
X = Not applicable

☐ J0 Connector and Shrouds

0 = No J0 connector
1 = 95 pin (19 x 7 position 17mm with shrouds)
X = Not applicable

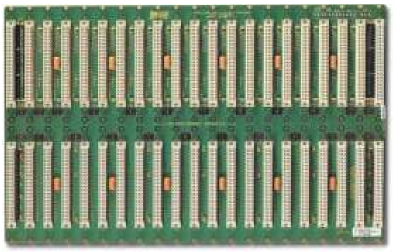
☐☐☐☐

Common Order Number Suffixes For Power & Shrouds

-0620	-0621
-1620	-0620R
-0621R	-1621

If an R is present at the end of the order#, the backplane is RoHS compliant.

* Long tails and shrouds cannot be used.



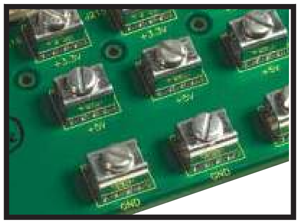
All Elma Bustronic VME backplanes are designed to maximize performance, minimize noise, and to give the customer the most reliable, cost-effective product possible. To achieve this we use 8-layer construction, stripline design, decoupling capacitors at every slot, inboard terminators, heavy power and ground planes, transient analysis simulation programs, and years of experience designing, building, and using backplanes. Three 2 oz. copper ground layers are used to fully shield the backplane to minimize RFI/EMI emission/susceptibility, to minimize crosstalk, and to maximize power

The outer ground layers serve to prevent signals or VCC from being exposed where they could be shorted or damaged. Two 2 oz. copper VCC layers are used to maximize power distribution and to act as virtual ground planes for the signals in order to minimize noise and crosstalk. The high frequency decoupling capacitors at every slot and distributed low frequency electrolytic capacitors throughout the board also help this effort. Measured results verify that Elma Bustronic backplanes are among the quietest in the industry.

Power Distribution

The versatile power distribution consists of power bugs at every other slot, an optional busbar may be installed directly across the power bugs without interfering with the mounting holes. In lieu of power bugs, studs may be installed. A 16-pin Molex connector is provided for power distribution and to provide control signal interfacing. High frequency decoupling capacitors are provided at every slot while low frequency decoupling is distributed throughout the PCB.

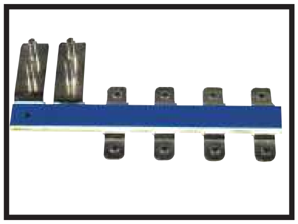
Power Bugs



Signal Layout

Onboard and inboard terminators are provided to reduce signal length and reduce possible signal reflections. A minimum stub length is utilized in routing and interconnecting to the terminators. The bus grant jumpers are arranged between each slot and are centered for easy installation and removal. All bus grant jumpers are accessible from the front and rear. Elma Bustronic backplanes have been designed with the customers' system designs in mind in order to give the highest performance, reliability, and value in the industry.

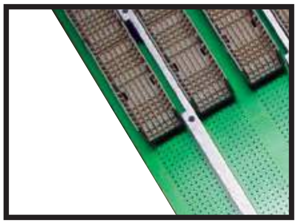
Busbar - Optional



Automatic Daisy Chaining

Automatic daisy chain eliminates a major source of problems when configuring a VME system, while eliminating the need for access to the backplane.

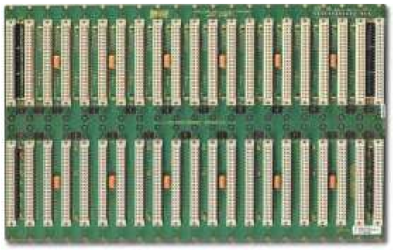
Stiffener - Optional



Mechanical Design

All mounting holes have adequate clearances for installation with metal hardware. All corners are rounded to allow installation into tight enclosures and prevent cables and wiring from snagging on the sharp corners. Power bugs and connectors are positioned to allow shrouds at each connector location for both J1 and J2. All slots and components are identified with easy to read silkscreen in yellow. A high quality soldermask is used to prevent chipping or scratches.

For more information see VME Reference Sheet at http://www.elmabustronic.com/CatalogInfo



Features

- Exceeds ANSI/VITA 1-1994 (R2002) and IEEE 1014-1987 specification
- Computer simulations utilized for design optimization
- Onboard, inboard termination
- Outer ground layers for mechanical protection and EMI/RFI shielding
- Optional BUSGRANT/IACK daisy chain connectors
- Optional high current busbar set
- Options for compliance to VITA 1.7 Increased Current Specification
- J2 Development backplanes with all J2 B row power and ground pins connected

Mechanical Specifications

Type	Slots	Height
J1+J2 Monolithic	2-21	6U
J1, J2, J3	3-21	3U
J2, J3 Development	2-21	3U
J2, J3 Overlays	3-6	3U

Electrical/Operating

Operating Temperature:
–40˚C to +85˚C
Storage Temperature:
–55˚C to 85˚C

Board Specifications

Type	Layers	2 oz. Copper Power & Ground	PCB UL Recognized 94V-0	PCB FR-4 or Equivalent	PCB Thickness
J1+J2 Monolithic	8	Yes	Yes	Yes	.125"
J1, J2, J3	8	Yes	Yes	Yes	.125"
J2, J3 Development	2	Yes	Yes	Yes	.125"
J2, J3 Overlays	4	Yes	Yes	Yes	.125"

Order Information

101VME □□□□ - □□□□

□□ Form

M1 = Monolithic, 6U
J1 = 3U, J1
J2 = 3U, J2
J3 = 3U, J3

□□ Slots

02-21

□ Power Interface

0 = 10 pin power tap with 6/32 screw
1 = M4 threaded stud
2 = 10 pin power taps with busbar kit
8 = Not applicable
9 = Custom (-9XXX sequential Numbers)

□ J0 and J1 Connector Tail Length if Applicable

0 = 13mm first and last slots, 6mm all other slots
1 = 17mm first and last slots, 6mm all other slots
2 = 6mm all slots
3 = 13mm all slots
4 = 17mm all slots
5 = 13mm first and last slots, 6mm ADC all other slots
7 = 96 pin, 6mm earless DIN
9 = Not applicable
C = 96 pin, 6mm with ADC

□ J2 and J3 Connector Tail Length if Applicable

0 = 96 pin, 13mm all slots
1 = 96 pin, 17mm all slots
2 = 96 pin, 6mm all slots
X = Not applicable

□ Shrouds

0 = All slots shrouded where applicable
1 = No slots shrouded
2 = All J2 slots shrouded
5 = J2, first and last slots
6 = Locking shrouds where applicable
7 = Locking shrouds J2 only

□□□□

Common Order Number Suffixes For Power & Shrouds for J1+J2 Monolithic

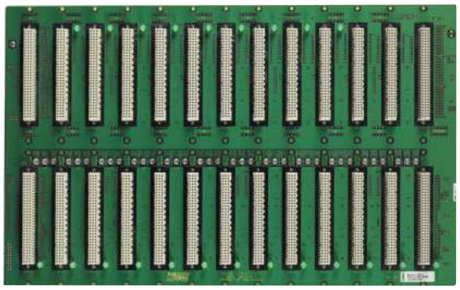
-0000	-0221	-0500
-0000R	-0221R	-0500R

Common Order Number Suffixes For Power & Shrouds for J1,J2, J3

-0000	-0500	-0590
-0900	-0000R	-0500R
-0590R	-0900R	

If an R is present at the end of the order#, the backplane is RoHS compliant.

VXI Backplanes



Features

- Compliant with VXIbus spec. Rev. 1.4-1992
- 10-layer, controlled impedance stripline design
- Electronic BUSGRANT, IACK daisy chain
- Superior power distribution
- Matched propagation delays
- Virtually zero crosstalk

Mechanical Specifications

Size	Slots	Height	Pitch
C Size	5, 6, 8, 9 and 13	6U, 9U	1.2”
D Size	5, 6, 8, 9 and 13	6U, 9U	1.2”

Board Specifications

Layers	2 oz. Copper Power & Ground	PCB UL Recognized 94V-0	PCB FR-4 or Equivalent	PCB Thickness
10	Yes	Yes	Yes	.125”

Electrical/Operating

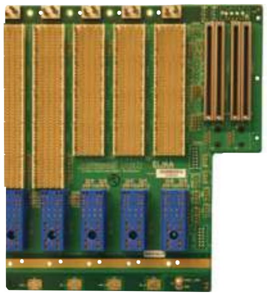
Conforms to:
Operating Temperature:
–40˚C to +85˚C
Storage Temperature:
–55˚C to 85˚C
Single Line Impedance:
55 Ohms +/- 10%
Max. Voltage Drop for +5V:
<40mV

The Elma Bustronic VXIbus backplane series are designed to fully comply with the VXIbus specifications, Rev. 1.4-5/92. Elma Bustronic has incorporated a feature set that is unique in the industry: a custom, laminated busbar, active or passive terminations, automatic active BUSGRANT and IACK jumpering, and optional AMP enhanced Eurocard connectors are offered, along with a 4-point chassis ground that can be modified by the user to isolate the chassis ground from the digital ground.

For more information see VME Reference Sheet at http://www.elmabustronic.com/CatalogInfo

Order Information

Slots	Height in.	Height mm	Width in.	Width mm	Order Number
C/05	10.317	262.100	7.000	177.800	101VXIM105
C/06	10.317	262.100	8.200	208.300	101VXIM106
C/08	10.317	262.100	10.600	269.200	101VXIM108
C/09	10.317	262.100	11.800	299.700	101VXIM109
C/11	10.317	262.100	14.200	360.680	101VXIM111
C/13	10.317	262.100	16.600	421.600	101VXIM113
D/05	15.567	395.400	7.000	177.800	101VXIM205
D/08	15.567	395.400	10.600	269.200	101VXIM208
D/13	15.567	395.400	10.600	421.600	101VXIM213



AdvancedTCA was a major initiative from PICMG, with over 125 members participating. The 8U x 280mm cards and 1.2” pitch allow a wealth of processors and components to be used. The technology utilizes primarily Dual Star (two hubs slots with direct links to each of the node slots) and Mesh switched fabric topologies (each slot acts as a hub slot, with direct links to every other slots, vastly increasing the bandwidth). The architecture will be able to handle interfaces up to 40Gpbs (for Terabit backplane bandwidth), High Availability (99.999% uptime), and Quality of Service issues demanded by the telecom central office. The backplane allows for 48VDC input from an external source to be distributed to the individual slot cards.

The ATCA backplane is broken up into zones. Zone 1 contains the power connector. Zone 2 is made up of the signal connectors carrying the base interface, clocks, update channel interface and the fabric interface. The base interface uses an Ethernet Dual Star topology. Horizontally the connector columns have 5 differential pairs and vertically there are 10 rows. The ZD connector is specifically designed for high speed differential signaling, and is capable of speeds up to 5 Gbps. Zone 3 is for Rear Transition Modules.

ATCA boasts the following:

- High speeds scalable to 2.5Tb/sec.
- High Availability RAS (Reliability, Availability and Serviceability) functionality by virtue of Redundancy, Failover, Fault prediction and prevention
- Open standards
- Interoperable third party products contributing to a dynamic ecosystem
- Robust system management features
- Scalable and cost effective

ATCA Topologies

AdvancedTCA specification allows a variety of architectural implementations. The topologies of the specification are Dual Star, Dual Dual Star, and Mesh (including Replicated Mesh). All of these configurations can go up to 14 slots (in a 19” rack). The channel mapping allows a standard ATCA switch card to support any configuration. For instance, a Dual Star (redundant hub slots running the fabric) implementation could be implemented with cards at either end of the subrack, adjacent in slots one and two or in the middle of the backplane.

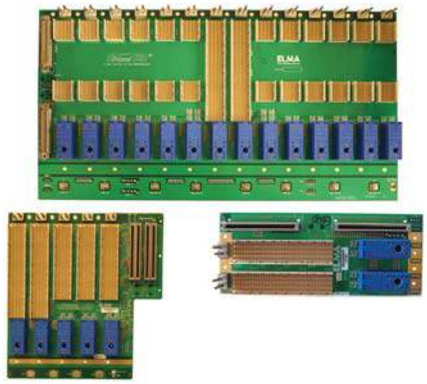
The topology of the ATCA backplane can greatly affect the overall system cost as the cards, backplane, etc, will be affected. Focusing on the backplane, a Mesh topology can demand significantly more layers than a Dual Star topology. With more point-to-point links, more layers need to be added to achieve the signal routing, which increase the cost of the backplane.

ATCA Routing

The routing of the 5-slot Mesh ATCA backplane is made up of 15 channels on each slot. Each channel has eight differential pairs and is designed as a XAUI link, which can run up to 10 Gbps (verified during signal integrity testing). Four channels from each slot create a full mesh, and using 12 channels a 3X Mesh can be implemented. Therefore, there are 3 XAUI connections between each of the slots. The 3 extra channels were routed between slots 1, 2, 3 and 4. In summary, there are a total of 4 channels connecting slots 1-4 and 3 channels connecting all 5 slots. See pinout diagram below for details. The 2-slot ATCA has direct point-to-point links between the two slots. See diagram below for details.

40G ATCA Efforts

The ATCA community has been moving to 10Gpbs per channel for 40G speeds. With Elma Bustronic’s extensive pre-layout and post-layout simulation studies, our backplanes have been fine tuned to achieve excellent performance. Our 40G ATCA backplanes are based on the design principles of IEEE 802.3-2008 and IEEE 802.3ba-2010 (10GBASE-KR and 10GBASE-KR4)

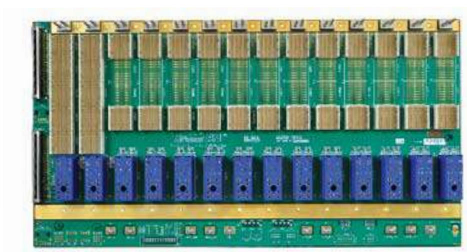


Dual Star and Mesh Features

- Compliant to PICMG 3.0 R2.0 specification
- Gigabyte/Terabyte per second bandwidth per shelf
- Connections to IPM Sentry shelf manager
- Controlled impedance stripline design
- Dual Star version has 2 Fabric slots, 12 node slots (other sizes available)
- Dual Star version has 2 shelf manager connectors in slot 0, allows full 14 slots
- Mesh versions fully connected
- 2-slot Mesh is point-to-point links, switchless

The Elma Bustronic 14-slot Dual Star AdvancedTCA (ATCA) backplanes are compliant to the PICMG 3.0 Rev.1.0 specification. The experts in high-speed differential pair routing, Elma Bustronic's ATCA backplanes have been simulated and characterized by our signal integrity lab to optimize performance.

The Elma Bustronic Mesh AdvancedTCA (ATCA) backplanes are compliant to the PICMG 3.0 Rev.1.0 specification. The experts in high-speed differential pair routing, Elma Bustronic's ATCA backplanes have been simulated and characterized by our signal integrity lab to optimize performance.



40G Features

- Compliant to PICMG 2.9 R1.0 specification
- Designed to meet 40Gbps (4 x 10G ports) data rates
- Based on design principles of IEEE 802.3ba-2010, 10GBASE-KR, and 40GBASE-KR4
- Nelco 4000 13-SI high grade laminate material
- Extensive pre-layout and post-layout simulation studies
- Backdrilled to minimize stub reflections
- Very low Insertion Loss Deviation (ILD)
- Dual shelf managers in slot 0, radial IPMB/I^{2}C implementation
- Up to 400W/slot 48VDC distribution to each slot
- 18 layer stripline design
- Test reports available upon request

Elma Bustronic's 40G ATCA backplane was tested at AdvancedTCA Interoperability Workshops (AIW) with leading board vendors 40G switch and payload cards. The backplane performed superbly, without dropping any packets or other issues.

Mechanical Specifications

Version	Height	Slots	Pitch
Dual Star	5U	14 (other sizes available)	1.2"
Mesh	5U, 7U	2, 5, 6, 14, and 16 slots	1.2"
40G	5U	14	1.2"

Board Specifications

Version	Layers	2 oz. Copper Power & Ground	PCB UL	PCB FR-4 or Equivalent	PCB Thickness
Dual Star	16	Yes	Yes	Yes	.132"
Mesh	10 layers (2-slot) 18 layers (5,14, 16 slot) 26 layers (6-slot)	Yes	Yes	Yes	.137" (2-slot) .151" (5-slot) .171" (6-slot) .136" (14-slot) .125" (16-slot)
40G	18	Yes	Yes	Nelco 4000 13-SI	.146"

Electrical/Operating

Conforms to:
Operating Temperature:
–40˚C to +85˚C
Storage Temperature:
–55˚C to 85˚C
Differential Impedance:
100 Ohm +/- 10 %

Order Information

109 □□□□ □ □□ - □ □ □ □

□□□□ Type

ATCA = AdvancedTCA

□ Form

5 = 5U, Zones 1 & 2
7 = 7U

□□ Slots

02-14

□ Topology

0 = Dual Star
1 = Dual-Dual Star
2 = Mesh
3 = Replicated Mesh

□ Channels

0 = Full channel

□ System Management

0 = Redundant shelf managers

□ Data Rate

0 = 3.125 Gbps
1 = 5 Gbps
2 = 6.25 Gbps
3 = 10 Gbps
4 = 25 Gbps

Standard Base Backplane Order#'s

Slots	Fabric Slots	Node Slots	Description	Order Number (Base)
14	2	12	5U Dual Star standard	109ATCA514
14	2	12	5U Dual Star 40G	109ATCA510-0003R
2	all	all	5U Mesh	109ATCA502
5	all	all	5U Mesh	109ATCA505
6	all	all	5U Mesh	109ATCA506
14	all	all	7U Mesh	1900001778
16	all	all	7U Mesh	1900001495

Features

- Complies to MicroTCA.0 Specification Rev 1.0
- Slot to slot aggregate bandwidth of 5,000 Mbytes/sec
- Accepts both single and double modules
- Compression-mount standard
- Optimized via signal integrity studies, reports available upon request
- Other versions available in various configurations - compact and mid size, cube and MicroSlim style
- MicroSlim version comes in horizontal mount orientation

Mechanical Specifications

Version	Height	Slots
Star**	3U	11 AMC, 1 MCH,1 JSM (J-TAG Switch Module) and 1 Power Module slot (all full size)
Dual Star**	3U	10 AMC, 2 MCH, 2 Power Module slot (all full size)
MicroSlim**	1U, 3U	6 AMC, 1 PM (Power Module), 1 MCH (MicroTCA Carrier Hub), 1 JSM (J-TAG Switch Module) and 2 CUs (Cooling Units)

**Compression-mount connectors standard

Electrical/Operating

Operating Temperature:
–40˚C to +85˚C
Operating Temperature:
–55˚C to 85˚C
Differential Impedance:
100 Ohm +/- 10 %

Board Specifications

Version	Layers	2 oz. Copper Power & Ground	PCB UL Recognized 94V-0	PCB FR-4 or Equivalent	PCB Thickness
Star	26	Yes	Yes	Yes	.195”
Dual Star	26	Yes	Yes	Yes	.195”
MicroSlim	20	Yes	Yes	Yes	1U, .167” 3U, .195”

Order Information

109 □□□□ □ □□ - □ □ □ □ □

□□□□ Type

MTCA = MicroTCA.0

□ Form

S = Single Width
M = Double Width

□□ Slots

02-14

□ Topology

0 = Single Star (1 MCH)
1 = Replicated Single Star (1 MCH)
2 = Dual Star (2 MCH)
3 = Mesh (2 MCH)
9 = Custom

□ Power

1 = 1 Power Module Slot
2 = 2 Power Module Slots

□ Connector Type

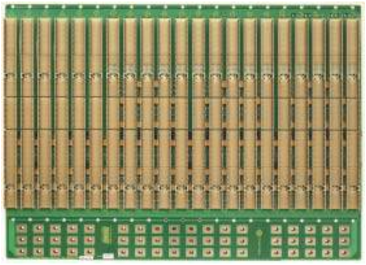
0 = Pressfit
1 = SMT
2 = Compression

□ Spacing

0 = Full Size
1 = Compact
2 = Midsize

Standard Base Backplane Order#’s

Height	Slots	Description	Order Number
3U	14	12 AMC, 1 power, 1 MCH slots all in full size	109MTCAS14-0100R
3U	14	12 AMC, 2 power, 2 MCH slots, all in full size	109MTCAS14-2220R
1U	9	Passive: 6 AMC, 1 PM, 1 JSM, 1 MCH, and 2 CUs (Cooling Units)	1900001880-0000R
3U	24	Passive: 12 AMC, 4 HDD (w/SATA), 2 PM 2 MCH, 1 JSM, 3 spare slots and 2 CUs (Cooling Units)	1900001881-0000R
1U	24	Active: 6 AMC, 1 PSU connector, 1 MCH, and 2 CUs (Cooling Units)	109MTCAS07-0122



The Elma Bustronic CompactPCI backplane series conform to the PICMG basic specification 2.0 R3.0 and Hot Swap specification 2.1 R1.0. The H.110 CT versions also conform to PICMG H.110 Computer Telephony Specfication 2.5 R1.0. We provide all standard features required for full compatibility, including all pin connections for bussed signal lines and all defined power and ground pins connected to their respective planes. User-defined VI/O is standard. 66Mhz versions are limited to 5 slots. 33Mhz versions are limited to 8 slots (without bridges).CompactPCI backplanes with slot counts beyond 8 have optional cPCI bridges (see cPCI Bridge section for details).

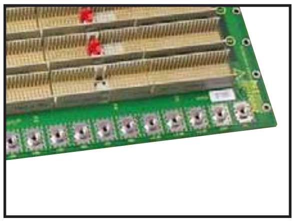
All Elma Bustronic backplanes are designed to maximize performance, minimize noise, and give the customer the most reliable, cost-effective products possible. We incorporate a full stripline design, generously distributed high and low frequency decoupling capacitors, 2 oz. power and ground planes to minimize noise. Our standard design with two 2 oz. copper ground planes fully shield the backplane, minimize EMI/RFI emissions susceptibility, minimize crosstalk, and maximize power distribution. There is also a full VI/O plane. Measured results verify that Elma Bustronic backplanes are among the quietest in the industry. We use stripline construction to assure the highest possible performance. By exclusively utilizing stripline construction, we eliminate a significant source of EMI/RFI radiation and give all signals similar characteristic impedances and minimal signal skew. All these items allow for significantly higher data transfer rates, since signal skew factors into the data transfer rate calculations four times.

For more information see cPCI Reference Sheet at http://www.elmabustronic.com/CatalogInfo

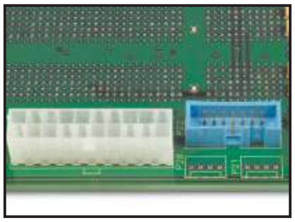
Power Distribution

The Elma Bustronic CPCI backplane family is designed with the power insertion area beside the signal slots, allowing for easy and efficient system integration. Adequate numbers of 6/32 nuts and an ATX connector have been inserted in this area to accommodate more power than the 28 amps required per slot. The ATX connector allows for an ATX power supply to be plugged in. The connector has 20 pins standard on our 6U CPCI backplane. The fastons have been added to allow additional power while taking a minimum of space. The blades are rated at 12A each. The Low Profie CPCI backplanes forego the power nuts for power studs between the slots. This method saves a slot width of space. The power bugs and taps are rated at 22A per connection.

Power Nuts



ATX + Utility



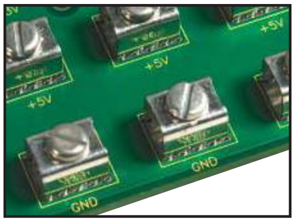
Signal Layout

The Elma Bustronic design conforms to the PICMG basic specification 2.0 R3.0 and basic Hot Swap specifications 2.0 R1.0. A minimum stub length is utilized in routing and interconnecting to the signal traces. Our design techniques avoid crosstalk and noise caused by inadequate ground and power. Every Elma Bustronic backplane is designed with the customer's system in mind—ensuring the highest performance, reliability, and value.

Jumpering

Jumpers can be installed to close a circuit. The backplane has labeled areas for jumper installation. The following applies to all of Elma Bustronic's CompactPCI and H.110 backplanes in 2-8 slot sizes. Configurations with 2-5 slots have an addition jumper consideration, the M66EN# jumper.

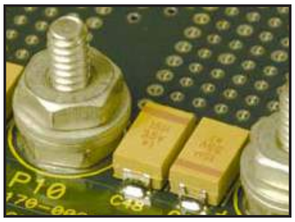
Optional - Power Bugs



64-EN# Jumper

If the jumper is installed, 64-EN# P2-B5 (see Hot Swap specification, PICMG 2.1) is ground, and 64-bit boards will initialize for 64-bit operation. If the jumper is not installed, 64-EN# is open, and 64-bit boards will initialize for 32-bit operation.

Optional - Power Studs



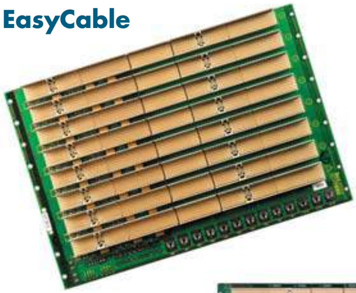
PS-ON# Jumper

If the jumper is installed, pin 14 PS-ON# on the ATX power connector is grounded. The ATX power supply will turn on immediately when plugged in. If the jumper is not installed, pin 14 PS-ON# on the ATX power connector is open. The ATX power supply will not turn on when plugged in. The PS-ON# jumper pins may be used to wire an on/off switch for the power supply.

2-5 Slot Backplanes Only: M66EN# Jumper

If the jumper is installed M66EN# P1-D21 is ground and the backplane operates in 33MHz mode. If the jumper is not installed M66EN# is bussed and the backplane operates in 66MHz mode.

EasyCable



32-Bit

EasyPlug

Low Profile

Features

- Conforms to PICMG basic specification 2.0 R3.0
- PICMG Hot Swap specification 2.1 R1.0
- Controlled impedance stripline design
- Virtually zero crosstalk
- Logical slot #1 (system controller) is right justified (left justified optional)
- EasyCable version has power studs on side of backplane, allowing for easier cabling
- EasyPlug version has 47-pin power connectors in either vertical or horizontal configurations
- H.110 versions conform PICMG Hot Swap specification 2.1 R1.0 PICMG H.110 Computer Telephony specification 2.5 R1.0
- Low profile versions have power studs between slots to save space
- 32-bit versions offer more I/O pins than the 64-bit version, where those pins are defined

Mechanical Specifications

Version	Height & Slots
EasyCable	3U - 4, 6, 8 slots 6U - 3, 4, 5, 6, 8 slots
EasyPlug	3U - 8 slots 6U - 8, 14, 16 slots 9U - 2, 4, 6, 8 slots
Low Profile	3U - 3 slot 6U - 4, 6, 8 slots
32-Bit	3U - 3, 8 slots 6U - 6, 8 slots

For 16 and 21 slot version: separate bridgeable segments

Board Specifications

Version	Layers	2 oz. Copper Power & Ground	PCB UL Recognized 94V-0	PCB FR-4 or Equivalent	PCB Thickness
EasyCable	8, 12 for H.110	Yes	Yes	Yes	PCB .125” thick (.132” thick for H.110)
EasyPlug	8, 12 for H.110	Yes	Yes	Yes	PCB .125” thick (.132” thick for H.110)
Low Profile	10-layers, 8-layers (2-slot) PICMG 2.16 versions vary	Yes	Yes	Yes	PCB .134” thick, (.125”) 2-slot, (.140”) 3-slot, PICMG 2.16 versions vary
32-Bit	10	Yes	Yes	Yes	PCB .125” thick (.128” for 3U 3-slot)

Electrical/Operating

Operating Temperature:
–40˚C to +85˚C
Storage Temperature:
–55˚C to 85˚C
Z0 Impedance (without connectors & daughter cards):
65 Ohm +/- 10%
Current Carrying Capacity (+3.3V/GND):
10A / slot

EasyCable Order Information

102CPCI ☐☐☐ - ☐☐☐☐☐

Form

3 = 3U
6 = 6U

Slots

04 = 4 slots 66mhz capable
05 = 5 slots 66mhz capable
06 = 6 slots
08 = 8 slots

Power Interface

0 = Power taps with 6-32 screws
1 = Not applicable
2 = 6-32 nuts and fastons for +12V, -12V (This is the only power interface for 3U backplanes)
4 = 6/32 pressed nuts, ATX connector and utility connectors
5 = ATX connector only, PWR taps +3.3V, 5V, V10, GND
6 = Power taps, ATX connector and utility connectors
9 = Custom (9XXX sequential numbers)
X = Not applicable

Connectors for P1, P2

0 = P1 short, P2 long
1 = P1 short, P2 short
2 = P1 short, No P2
X = Not applicable
7 = 96 pin, 5mm without shrouds, all slots
X = Not applicable

Connectors for P3, P4 & P5

0 = Not applicable
1 = Not applicable
2 = Not applicable
3 = Not applicable
4 = Not applicable
5 = P3 & P5 long type AB, P4 long type A
X = Not applicable

Shrouds

0 = P2 only
1 = Not applicable
2 = Not applicable
3 = Not applicable
4 = Not applicable
5 = Not applicable
6 = Not applicable
7 = P2 if long tail, P4 type A , P3 & P5 type AB
X = Not applicable

Common Order Number Suffixes For Power & Shrouds

-4057	-4057R
-4157	-4157R
-40X0	-40X0R
-41XX	-41XXR

If an R is present at the end of the order#, the backplane is RoHS compliant.

EasyPlug Order Information

103 ☐☐☐☐☐☐☐ - ☐☐☐☐

Type

CPCI = CPCI Backplane, 64 Bit
CTEL = H.110 compatible, 64 Bit
CPCR, CTER = 64 Bit, system slot right
CPCL = 64 Bit, system slot left
CP3R, CT3R = 32 Bit, system slot right
CP3L, CT3L = 32 Bit, system slot left

Form

3 = 3U
6 = 6U
7 = 7U
9 = 9U

Slots

01-21

Power Interface

0 = Power taps with 6-32 screws
1 = 3 Positronic connectors for 6U power supplies
2 = 6-32 nuts and fastons for +12V, -12V*
3 = 1 Positronic connector for 3U power supply
4 = 2 Positronic connectors for 3U power supplies
5 = 3 Positronic connectors for 6U power supplies
6 = 1 Positronic connector for 6U power supply
7 = 2 Positronic connectors for 6U power supplies*
8 = 4 Positronic connectors for 3U power supplies
9 = Custom (9XXX sequential numbers)
X = Not applicable

Connectors for P1, P2

0 = P1 short, P2 long
1 = P1 short, P2 short
2 = P1 short, No P2
X = Not applicable

Connectors for P3, P4 & P5

0 = Not applicable
1 = Not applicable
2 = Not applicable
3 = P3 long type AB, P4 tye A long all slots, P5 long type AB for CTEL
4 = P3 long type AB, P4 short (slot 1 long), P5 long type AB for CTEL
5 = P3 & P5 long type AB, P4 long type A
X = Not applicable

Shrouds

0 = P2 only
1 = Not applicable
2 = Not applicable
3 = Not applicable
4 = Not applicable
5 = P2 if long tail, P4 type A all slots, P3 & P5 type AB for CTEL
6 = P2 if long tail, P4 slot 1 type A, P3 & P5 type AB for CTEL
7 = P2 if long tail, P4 type A , P3 & P5 type AB
X = Not applicable

Common Order Number Suffixes For Power & Shrouds

-21XX	-21XXR
-3157	-3157R
-1157	-1157R
-7157	-7157R

If an R is present at the end of the order#, the backplane is RoHS compliant.

Low Profile Order Information

105 □□□□ □ □□ - □ □ □ □

Type

CPCI = CPCI Backplane, 64 Bit
CTEL = H.110 compatible, 64 Bit
CPCR, CTER = 64 Bit, system slot right
CPCL = 64 Bit, system slot left
CP3R, CT3R = 32 Bit, system slot right
CP3L, CT3L = 32 Bit, system slot left

Form

3 = 3U
6 = 6U
7 = 7U

Slots

02-21

Power Interface

0 = Power taps on GND, +5V, +3.3V, faston blades for +/- 12V
1 = Studs
9 = Custom (9XXX sequential numbers)
X = Not applicable

Connectors for P1, P2

0 = P1 short, P2 long
1 = P1 short, P2 short
2 = P1 short, No P2
X = Not applicable

Connectors for P3, P4 & P5

0 = Not applicable
1 = Not applicable
2 = Not applicable
3 = P3 long type AB, P4 short (slot 1 long), P5 long type AB for CTEL
4 = P3 long type AB, P4 long all slots, P5 long type AB for CTEL
5 = P3 & P5long type AB, P4 long type A
X = Not applicable

Shrouds

0 = P2 only
1 = Not applicable
2 = Not applicable
3 = Not applicable
4 = Not applicable
5 = P2 if long tail, P4 type A all slots, P3 & P5 type AB for CTEL
6 = P2 if long tail, P4 slot 1 type A, P3 & P5 type AB for CTEL
7 = P2 if long tail, P4 type A , P3 & P5 type AB
X = Not applicable

Common Order Number Suffixes For Power & Shrouds

-0136	-0157
-10X0	-1157
-11XX	-20X0
-0136R	-0157R
-10X0R	-1157R
-11XXR	-20X0R

If an R is present at the end of the order#, the backplane is RoHS compliant.

32-Bit Order Information

10 □ □□□□ □ □□ - □ □ □ □

Version

2 = EasyCable
5 = Low Profile

Type

CP3R = 32 Bit, System Slot Right
CP3L = 32 Bit , System Slot Left

Form

3 = 3U
6 = 6U

Slots

02-21

Power Interface

0 = Power taps on GND, +5V, +3.3V, faston blades for +/- 12V
1 = Studs
2 = Custom (9XXX sequential numbers)
X = Not applicable

Connectors for P1, P2

0 = P1 short, P2 long
1 = P1 short, P2 short
2 = P1 short, No P2
X = Not applicable

Connectors for P3, P4 & P5

0 = Not applicable
1 = Not applicable
2 = Not applicable
3 = P3 long type AB, P4 tye A long all slots, P5 long type AB for CTEL
4 = P3 long type AB, P4 short (slot 1 long), P5 long type AB for CTEL
5 = P3 & P5 long type AB, P4 long type A
X = Not applicable

Shrouds

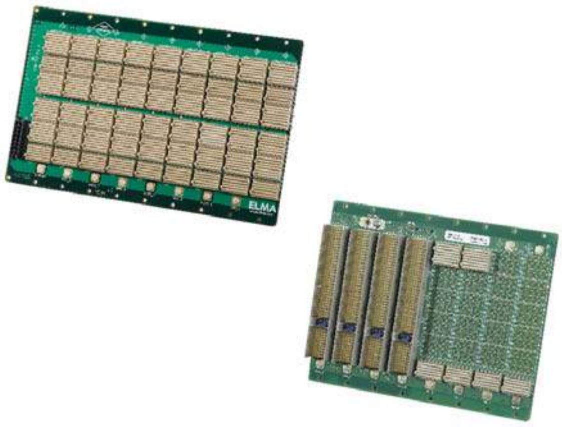
0 = P2 only
1 = Not applicable
2 = Not applicable
3 = Not applicable
4 = Not applicable
5 = P2 if long tail, P4 type A all slots, P3 & P5 type AB for CTEL
6 = P2 if long tail, P4 slot 1 type A, P3 & P5 type AB for CTEL
7 = P2 if long tail, P4 type A , P3 & P5 type AB
X = Not applicable

Common Order Number Suffixes For Power & Shrouds

-10X0	-11XX
-20X0	-10X0R

If an R is present at the end of the order#, the backplane is RoHS compliant.

cPCI Backplanes - Serial and Plus IO



Features Serial Backplane

- PICMG CPCI-S.0 R1.0 2011 CompactPCI Serial compliant Backplane
- 1 x CPCI S.0 System Slot (CPU) and 8 x CPCI S.0 Peripheral Slots
- High-speed connectors supporting up to Data Transfer rate up to 12Gbps are in all 9 Slots
- Designed to support Rear Transition Modules
- Single Star Topology for Serial Interfaces such as PCI Express, SATA, USB2 + USB3 are provided by the CPCI S.0 System Slot
- All 9 Slots are connected to each other through a Full Mesh Ethernet Topology
- Eurocard form factor in 3U height

Features Plus IO Backplane

- PICMG 2.30 CPCI PlusIO R1.0 2009 compliant backplane
- Hybrid function by having standard CPCI Standard Slots and CPCI – S.0 Peripheral Slots
- High-speed connectors in the 4 x CPCI S.0 Peripheral Slots, legacy cPCI in other 4 slots
- Eurocard form factor in 3U height
- Designed to support Rear Transition Modules
- System management interface on the backplane

Mechanical Specifications

Version	Height	Slots	PCB Thickness
Serial Backplane	3U	9	4.15mm
Plus IO Backplane	3U	4	4.3mm

Board Specifications

Version	Layers	Slot Pitch	PCB Material
Serial Backplane	TBD	0.8”	NELCO 4000-13
Plus IO Backplane	12	0.8”	FR-4 or equivalent

Order Information

Version	Height	Slots	Width	Order Number
Serial Backplane	3U	9	197.12mm	1900002441-0000
Plus IO Backplane	3U	4	160.56mm	TBD

Features

- Conforms to PICMG 2.16 R1.0 specification
- Conforms to PICMG basic specification 2.0 R3.0
- Moves data via switched Ethernet fabric (10/100/1000 Mbit/s)
- Hot-swappable fabric slots in various configurations
- Standard power studs
- Supports existing SBCs, Ethernet cards, and line cards
- 10-14 layer controlled impedance stripline design
- Versions with connections to IPM Sentry Shelf Manager

Mechanical Specifications

Height	Slots
6U	4, 6, 8, and 21 slot sizes standard

Ethernet and cPCI compatible

Board Specifications

Layers	2 oz. Copper Power & Ground	PCB UL Recognized 94V-0	PCB FR-4 or Equivalent	PCB Thickness
10-14	Yes	Yes	Yes	.132”, .152”

Electrical/Operating

Conforms to:
Operating Temperature:
–40˚C to +85˚C
Storage Temperature:
–55˚C to 85˚C

The performance of CompactPCI is vastly improved with the cPSB (PICMG 2.16) protocol. It provides the ideal solution for third-generation wireless, Internet protocol, voice over IP (VoIP), and other applications that require high processing power and data rates. CPSB increases system performance by moving data traffic off the shared bus, and onto an embedded switched Ethernet network fabric (10/100/1000 Mbit/s), accessed via the P3 connector.

The 4-slot, 6-slot, and (one of the) 8-slot backplanes have 1 fabric slot, with the rest of the slots as node slots with the CompactPCI bus. Elma Bustronic also offers an 8-slot version with 2 fabric slots, with the rest of the node slots with the CompactPCI bus and with or without the H.110 bus. All of Elma Bustronic’s standard PICMG 2.16 backplanes offer one slot that is convertible to a system slot via a CPU Enable jumper. With the power studs and power blades dispersed throughout key locations in the backplanes, the overall widths are a true 4-slot, 6-slot, and 8-slot size. This allows the 4-slot, and 8-slot backplanes to fit within 2U, and 4U horizontal chassis respectively. Further, the use of 6/32 power studs gives the backplanes modularity, allowing power interface boards in various configurations to be mounted to the backplane. Elma Bustronic offers design services for various other configurations of PICMG 2.16. The backplanes have several 6/32 power studs for 3.3V, 5V, VI/O, and GND and fast-on blades for +/- 12V. Per the specification, the shelf geographical addressing is located in the P3 section of the backplane and is configurable. The DEG (derate/degrade) and FAIL headers can be run from the power supply to the CPU board for power supply monitoring. A PRST (power on reset pin) is also included. Some cPSB versions include a 20-pin header with pins for the Intelligent Platform Management Bus (IPMB) for shelf management.

Order Information

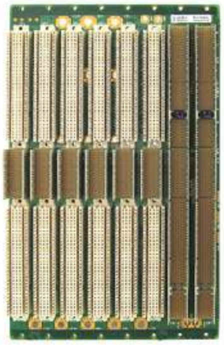
Slots	Fabric Slots	Node Slots	Height in.	Width in.	Order Number
4	1	2 w/cPCI, 1 node/sys slot w/ cPCI	10.32	3.16	107PS11604
6	1	4 w/cPCI, 1 node/sys slot w/ cPCI	10.32	4.78	107PS11606
6	1	4 w/cPCI and H.110 bus, 1 node/sys slot w/ cPCI	10.32	4.78	108PS11606
8	1	6 w/cPCI, 1 node/sys slot w/ cPCI	10.32	6.38	107PS11608
8	2	5 w/cPCI, 1 node/sys slot w/ cPCI, IPM Sentry shelf mgmt. connector	10.32	6.38	107PS21608
8	2	5 w/cPCI and H.110, 1 node/sys slot w/cPCI	10.32	6.38	108PS21608
21	2	19 node slots, no PCI	10.32	16.78	107PS21621

CompactPCI Express

- Complies to PICMG EXP.0 R1.0 specification
- PCI Express over 3U CompactPCI form factor
- System slot-two ZD and one enriched 2mm HM,power connector
- Type 2-one ZD and the one enriched 2mm HM
- The Type 2 slots can be converted to hybrid cPCI/PCIe
- Controlled-Impedance stripline design
- RoHS compliant versions also available
- 4-slot version uses power nuts, 6-slot version uses M4 power bolts

Order Number: 1900001476 (4-slot), 1900001737 (6-slot)

VITA 31.1



- 10/100/1000BASE-T Ethernet switched network on a VME64x backplane
- 2 redundant VITA 31.1 Fabric Slots, right side of backplane
- 6 VITA 31.1 Node Slots
- Increase bandwidth and reliability
- Switches 100% compatible to PICMG 2.16
- Standard VME64x / cPCI connectors
- Automatic active Daisy Chain
- Passive inboard termination (basic current consumption 1.5A)
- Power input: M3/M4 power bolts (M3/M4 cable lugs, washer and nuts enclosed)
- 10-layer construction
- ANSI/VITA 1.1-1997 VME64x Standard compliant
- According to VITA 1.7 Increased Current Level For 96 Pin & 160 Pin DIN/IEC Connector

Order Number: 1900001484

Miscellaneous Backplanes & Boards

- Backplanes in ISA, PXI, PCI-X, PCI, ISA and more
- ISA available in 4, 6, 8, 12 and 14 slots
- Busbar Kits – For VME, VXI, VME64x and custom applications. Can be cut to various sizes
- Daisy Chain Modules (Jumper Boards) – Fills unused slots in the system and deflects airflow. Available in various chassis depths and heights.
- VME J0 Connector Mounting Boards - in 2-21 slots. Completely user definable
- Terminators - VME J1 and J2 off-board terminators
- PXI, PCI-X Backplanes – See custom versions on PXI and PCI-X pages on Elma Bustronic's Web site

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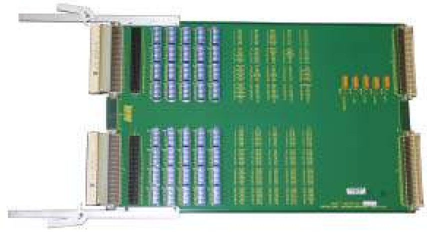
Rear Transition Module (RTM)

- For VXS, VME/64x, cPCI, ATCA, VPX and other architectures
- Elma Bustronic offers unique rear I/O and RTM solutions VXS and VPX
- Design and contract assembly services available
- Sizes in 3U x 80mm, 6U x 80mm, 8U x 80mm and more

Universal VPX RTM Breakout Board

- 6U x 80 mm RTM format
- Designed to meet VITA 46.10 for VPX RTM modules
- Supports 2 Level Maintenance per VITA 46.0 section 4.5
- 10-layer design
- Breakout for all signals possible depending upon connector configuration
- All the available RTM signals from connectors rJ0-rJ6 are broken out to .010" x .010" grids of solder pads
- Front panel and injector/ejector optional, with all necessary holes provided
- Strain relief holes provided directly behind the front panel mounting location for clamping bar or wire-ties



Features

- Designed to meet mechanical and electrical connection requirements of latest ANSI/VITA standards
- All J1 (and J2) connector pins can be individually switch isolated
- Test points for all 96 or 160 pins of J1 and J2
- Optional J0 connector available for VME64x
- Designed for use in 160mm and 220mm chassis
- Rugged card guide handles most legacy VME products

Board Specifications

VME, VXI - 8-layer stripline design
VME64x - 12-layer stripline design
PCB UL recognized 94V-0
PCB FR-4 or equivalent
PCB .062”

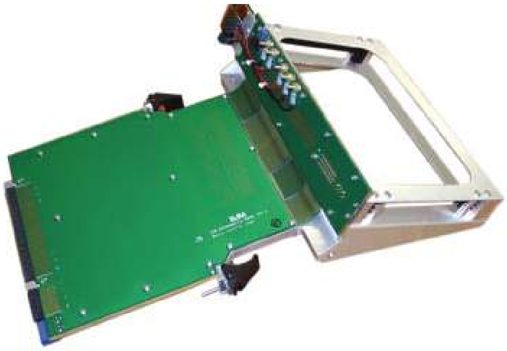
Mechanical Specifications

VME64x - 6U x 220mm
VME - Can be assembled in any combination to make 3U, 6U, 9U, or 12U configurations
VXI – 6U x 340mm
All J1, J2 and J0 connectors are DIN, class II

Elma Bustronic test extender boards comply with the mechanical and signal connection requirements of the latest ANSI/VITA standards. The extender boards are designed to bring a circuit card completely out of a card cage or enclosure so that it can be tested or debugged. This provides access to both sides of the test board. There are test points for all of the lines on each 96 pin (VME, VXI) or 160-pin (VME64x) connector. Each signal, power, and ground line can be individually isolated with the DIP switches. The extender boards accommodate use in 160mm and 220mm chassis. The rugged card guide handles securely hold the test board, ensuring a reliable connection. The +5U, ±12V, 3.3V, and GND pins for VME64x are tied to their respective planes.

ORDER INFORMATION

Type	Height	Length	Order Number
VME64x (no P0 connector)	6U	220mm	116EXT6122-012X
VME64x (with P0 connector)	6U	220mm	116EXT6122-0125
VME	3U	200mm	111EXT3122
VME	6U	200mm	111EXT6122
VME	9U	200mm	111EXT9122
VME	3U	400mm	111EXT3140
VME	6U	400mm	111EXT6140
VME	9U	400mm	111EXT9140
VXI	6U	340mm	113EXT6134-012X



Features - VXS, VPX

- Conforms to VITA 41.0 VXS or VITA 46 VPX backplane specifications
- Controlled impedance rigid-flex-rigid design
- Alignment keying headers provided for extender and plug-in card
- 100 Ohm differential pair routing
- J1 signals are single-ended signals and run point-to -point across the extender (VPX version)
- Mechanical frame supports 6U, 160mm plug-in card
- Signal rate: 3.125 Gb/sec
- Current monitor on +5V power (VXS version)
- **Order Number:** 118EXT6024-0XXX (Payload)
  115EXT6024-0XXX (Switch)
  119EXT6024-05XX (6U VPX)
  119EXT3024-07XXR (3U VPX)

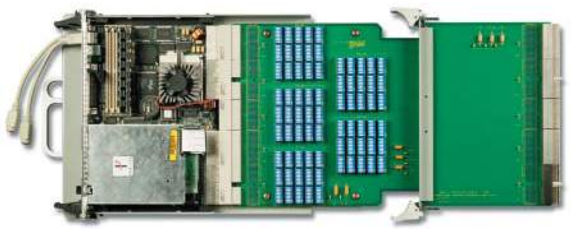
Board Specifications

10-layer stripline design
PCB UL recognized 94-V0
PCB Material: FR4 rigid, polyimide flex
PCB .080” thick

Mechanical Specifications

6U x 240mm

Test Extender Boards - cPCI, ATCA, uTCA



Shown with cPCI board inserted into the extender

Features - cPCI

- Designed to meet latest PICMG specification
- External ground planes for mechanical protection and EMI/RFI shielding
- IEEE 1101.10 compatible injector/ejector handles
- Test points for all lines on each 2mm HM connector in P1-P5 can be individually switch isolated
- Metal frame securely holds test board in place
- **Order Number:** 117EXT6116-0XXX

Board Specifications

12-layer stripline design (cPCI)
PCB UL recognized 94-V0
PCB FR-4 or equivalent
PCB .062" thick

Mechanical Specifications

6U x 400mm

Elma Bustronic CompactPCI test extenders comply with the mechanical and signal connection requirements of PICMG 2.0 Rev. 3.0. The cPCI extender boards bring a circuit card completely out of a card cage or enclosure so that it can be tested or debugged. This provides access to both sides of the test board. There are test points for all of the lines on each 2mm HM connector in P1-P5. Each line in rows A-E of the 2mm HM connector can be individually isolated with the DIP switches. The cPCI extender board accommodates use in 6U x 400mm chassis. The secure metal frame firmly holds the extender board to the test board. It also has ejector/injector latches, allowing the extender board to lock into the chassis.

Additional features include high and low frequency decoupling capacitors, five signal layers and seven power and ground planes. Elma Bustronic test extenders are designed to maximize perfomance, minimize noise and give the customer the most accurate test results possible.

Features - ATCA

- Mechanical extension of boards outside the chassis for testing
- Metal frame securely holds test board in place
- Designed to meet mechanical and electrical connection requirement of PICMG Rev. 3.0
- External ground planes for mechanical protection and EMI/RFI shielding
- The injector/ejector handles provide a secure and reliable connection to the chassis
- **Order Number:** 114EXT8040-0XXX

Board Specifications

10-layer stripline design
PCB UL recognized 94-V0
PCB FR-4 or equivalent
PCB .062" thick

Mechanical Specifications

8U x 711.2mm

The AdvancedTCA extender board extends both the power and IPMB (Intelligent Platform Management Bus) signals. With a 10-layer stripline design, the extender is designed for the full populated fabric slot (5 ZD connectors, P20 thru P24) and the power connector J10. The Zone 3 section is served by a blind board assembled to Zone 1+2 through the frame. The flexible design of the Zone 3 area allows for customization with minimum costs, by simply changing the blind board the required configuration. The complete keying system, including the Zone 3 area is assembled.

Features - uTCA

- Complies with MicroTCA.0, AMC.1 R1.0, AMC.2 D0.96A
- Extends board outside of the card cage for easy test or de-bug
- Extends all fabric signals, 3 clock lines
- Virtually zero power consumption
- Metal frame securely holds test board in place
- Virtually zero power consumption
- Management and payload power can be individually switch isolated
- **Order Number:** 026-505

Rear Extender Boards - cPCI

Features

- Compliant to PICMG 2.0 Rev. 3.0 specifications
- 6U x 180mm form factor
- Extends rear I/O signal
- 12-layer controlled impedance stripline design
- Injector/ejector latches provide easy insertion and removal
- PCB FR-4 or equivalent, 0.125" thick

Order Information

Type	Height	Length	Order Number
cPCI Rear	6U	180mm	117FFE6018-0XXX

Form Factor Extenders

Features

- Versions for VME, VME64x
- Allows boards of different depths to be used in the same depth card cage
- Outer ground planes for mechanical protection and EMI/RFI shielding
- Available in multiple sizes: 3U x 60mm, 6U x 60mm,
- 6U x 120mm, 6U x 180mm
- High performance stripline design

Order Information

Type	Height	Length	Order Number
VME	3U	60mm	111FFE3006-01XX
VME	6U	60mm	111FFE6006-012X
VME	6U	120mm	111FFE6012-012X
VME	6U	180mm	111FFE6018-012X
VME64x	6U	60mm	116FFE6006-012X
VME64x	6U	180mm	116FFE6018-012X
VME64x (w/ P0 connector)	6U	180mm	116FFE6018-0125

Features

- Conforms to electrical and mechanical connections latest VME, VME64x, cPCI, AMC or VPX specifications
- Verifies chassis can meet power requirement and specifications
- Aids in locating hot spots in the chassis
- Visual GO-NO GO indicators for +5V, +3.3V, +12V, -12V VME primary test points +V1, +V2, -V1, -V2, ACFAIL, SYSRESET, SYSFAIL, and GROUND
- CPCI primary voltage test points are V I/O, PRST#, FAIL#, and GND
- Power supply loading can be controlled with front panel switches

Developed to enhance testing of VME, VME64x, cPCI, AMC and VPX systems the load boards aid the system designer in assuring adequate chassis cooling and verifying that the chassis is capable of meeting the power requirements of the system (or VITA, PICMG specs). Predominantly used by chassis manufacturers and system developers, the load board provides significant time and expense savings by assuring a system's operating specifications. The load board functions to test a system's cooling capabilities by first applying the load to the power supply for verification and finally creating the necessary heat to confirm chassis cooling. By locating hot spots in the chassis, a system designer can verify where to optimally redirect the airflow to prevent overheating. The load board increases productivity by quickly and accurately characterizing systems at low cost. In addition, the cPCI load board offers power supply loading that utilizes binary switches to impose a load ranging from 0 to 7 amps of the primary load. This feature is also used for thermal characterization.

The AdvancedMC™ load board is dedicated for testing the cooling and power of MicroTCA systems. Single module/full size is standard with options for double modules and compact or mid sizes. The board is hot swap pluggable and has IPMI support. The load is configurable in to seven wattages: 0W, 20W, 30W, 40W, 50W, 60W and 70W. Six LEDs on the front panel indicate which power level is activated. If all LEDs are off, the power is 0W. Custom wattages and access management is available upon request.

CPCI Test Point Chart

Switch	+5V	+3.3V	+12V	-12V	V I/O:+5V	V I/O:+3.3V
000	off	off	off	off	off	off
001	1 A	1 A	0.1 A	0.1 A	5.0 A	3.3 A
010	2 A	2 A	0.2 A	0.2 A	2.5 A	1.7 A
011	3 A	3 A	0.3 A	0.3 A	7.5 A	5.0 A
100	4 A	4 A	0.4 A	0.4 A	1.3 A	0.8 A
101	5 A	5 A	0.5 A	0.5 A	6.3 A	4.1 A
110	6 A	6 A	0.6 A	0.6 A	3.8 A	2.5 A
111	7 A	7 A	0.7 A	0.7 A	8.8 A	5.8 A

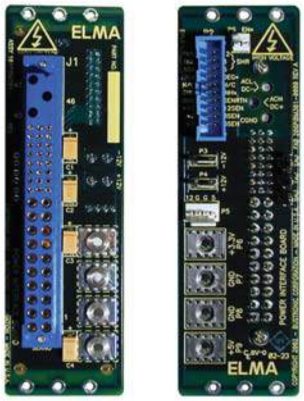
VME Test Point Chart

Switch	+5V	+3.3V	+12V	-12V
000	off	off	off	off
001	1 A	1 A	0.1 A	0.1 A
010	2 A	2 A	0.2 A	0.2 A
011	3 A	3 A	0.3 A	0.3 A
100	4 A	4 A	0.4 A	0.4 A
101	5 A	5 A	0.5 A	0.5 A
110	6 A	6 A	0.6 A	0.6 A
111	7 A	7 A	0.7 A	0.7 A

Order Information

Type	Height	Length	Order Number
AMC (uTCA)	3U	180mm	1940000264-0000
cPCI	6U	160mm	1940000135-0000
VME/VME64x	6U	160mm	1940000140-0000
VPX	3U	160mm	1940000345-0000R
VPX (convection-cooled)	6U	160mm	1940000355-0000R
VPX (conduction-cooled)	6U	160mm	1940000376-0000R

Power Interface Boards



Features
- Designed to comply with power interface specification PICMG 2.11 Rev. 1.0
- Designed to comply with IEEE 1101.10 mechanical specification
- 3U and 6U, one or two pluggable 47-pin power connectors
- Interface to backplane via power bugs with 6/32 screws
- Header for voltage sense, current share (2 ps connector version) and IPMB interface compliant to system management specification PICMG 2.9 Rev. 1.0
- Power taps for +5V, 3.3V, GND and faston blades for +12V, -12V
- Utility (20-pin), aux/disk drive, and power switch connectors
- Geographical Addressing on the power supply connector is selectable

The Power Interface Boards are separate boards for the power section of the backplane. They are used to facilitate pluggable power supplies, headers, and utility connectors. Elma Bustronic's standard backplane lines utilize power taps and power studs, which are wired to the power supplies. With the PIBs, customers will be able to choose between Elma Bustronic's standard power interface and pluggable modules. The power boards come in standard 3U and 6U heights and contain one or two 47-pin Positronic hot-pluggable power supply connectors (Positronic PCIH47F9300A1-246.0), and a 20-pin header for voltage sense and IPMB interface (Thomas & Betts 609-2037 or equivalent). Two power taps are for +5V, two for 3.3V, and four for GND. There are also four Fast-on blades each for -12V and +12V (AMP 63650-1 or equivalent). (For the 1 ps connector version, reduce the number of power taps and faston blades listed above in half.) The PIB interfaces to the backplane via power bugs with 6/32 screws. The design also includes mounting holes, allowing the PIB to be securely fixed to the chassis.

Other features include an auxiliary/disk drive connector (TYCO 350424-1 or equivalent), and a power switch header (AMP/TYCO 640456-2 or equivalent). The sense lines help the power supply better regulate the power at the load end. The function header allows remote or local sense. For optimal power regulation, remote sense is recommended. The current share lines allow multiple power supplies to share current, either on one PIB (with two power supply connectors) or between multiple PIBs. The current share lines have to be connected if using more than one PIB. The Geographical Addressing is configurable through jumpers, with GAO, GA1, and GA2. (The 2 ps version has two sets of these jumpers.) The IPMB interface is compliant to system management specification PICMG 2.9 Rev. 1.0. The PIB is also designed to comply with the power interface specification PICMG 2.11 Rev. 1.0 and with the IEEE 1101.10 mechanical specification.

Order Information

Height	Width	Power Supply Connectors	Order Number
3U	1.54”	single	106PIMB301-0000
3U(w/ AC pins)	1.54”	single	106PIMB301-9001
3U	3.13”	dual	106PIMB302-0000
3U(w/ AC pins)	3.13”	dual	106PIMB302-9001
6U	1.54”	single	106PIMB601-0000
6U(w/ AC pins)	1.54”	single	106PIMB601-9001
6U	1.54”	dual	106PIMB602-0000
6U(w/ AC pins)	1.54”	dual	106PIMB602-9001

Bridges - cPCI

- Low profile bridge enables the use of off-the-shelf rear transition modules
- Based on the Pericom P17C8154 PCI to PCI Bridge
- Compatible with the Intel 21154BE/AC/AE/BE and P21150 drivers
- Allows concurrent bus transfers on both PCI bus segments
- Accepts 32-bit or 64-bit, automatic detection of bus widths
- Accepts 33MHz or 66MHz bus frequencies
- Supports 3.3V or 5V input for bridge driver (onboard voltage regulator)
- Provides 7 clock signals for the secondary backplane
- Arbitration for 7 devices on the secondary backplane possible
- Version available for right or left-justified system slot

System Configuration

- The bridge spans 4 slots
- System configurations with one bridge: 7 slot (primary) + 3-7 slot (secondary) backplane
- System configurations with one bridge: 7 slot (primary) + 7 slot (middle) +3-7 slot (tertiary) backplane. The configurations are for 33 MHz operation-fewer slots are supported with 66 MHz operation.

Order Information

Height (mm)	Width (mm)	Thickness (mm)	Order Number
95.13	74.81	1.8	1940000260-0000R (Left)
95.13	74.81	1.8	1940000260-0001R (Right)

System Monitor OnlinePro

- Up to 8 voltages
- Monitors up to 14 temperature sensors
- Monitor and control up to 12 fans
- Ethernet interface: TCP/IP HTTP, Telnet protocol supported
- RS232 interface
- User configurable I/O pins

The SysMon OnlinePro is a platform independent system monitor for monitoring internal system conditions including temperature, voltage, fan rotation or power supply. The system monitor uses a 16-bit microcontroller with integrated 12-bit A/D converter. It has also a built-in web page allowing the user to monitor the system operation from any place with Internet connectivity. For fans with PWM regulation only!

Order Information

Height	Width	Order Number
3U	TBD	024-974

Voltage Monitor - VME, VXI

- Monitors the status of +5V, +12V, -12V Remote LED display board with ribbon cable
- Over/Under voltage display format
- Compact size (approx. 4.0” x 1.5”)
- Out-of-tolerance “FAIL” output

Order Information

Height	Width	Order Number
4.0 in	1.5 in	1940000009

VPX Cabling System

- Direct connection alternative to RTM solutions for VPX
- Compatible with the latest VITA 46.0 specifications
- For use in deployed or development/test applications
- Pulls signals from slot to slot and/or chassis to chassis with virtually zero signal degradation
- Fully scalable & stackable to meet application needs
- Versions for either front or rear backplane plugging
- Plug directly into backplane to SMA or other contacts for signal test setups
- Resistant to shock and vibration
- Can be used for out-of-band communication

The VPX cabling system is the industry's first direct cabling system for the VPX architecture. Compliant to the latest VITA 46 and VITA 65 specifications, the cabling system can be used for I/O to bulkhead connectors, slot-to-slot connections, and out-of-band communication. The cabling solution can also be used for system development. The direct cabling system also has front-plug versions, which allow testing across the backplane or full interconnect path.

Order Information

Contact factory for order information.

SerDes Test Devices

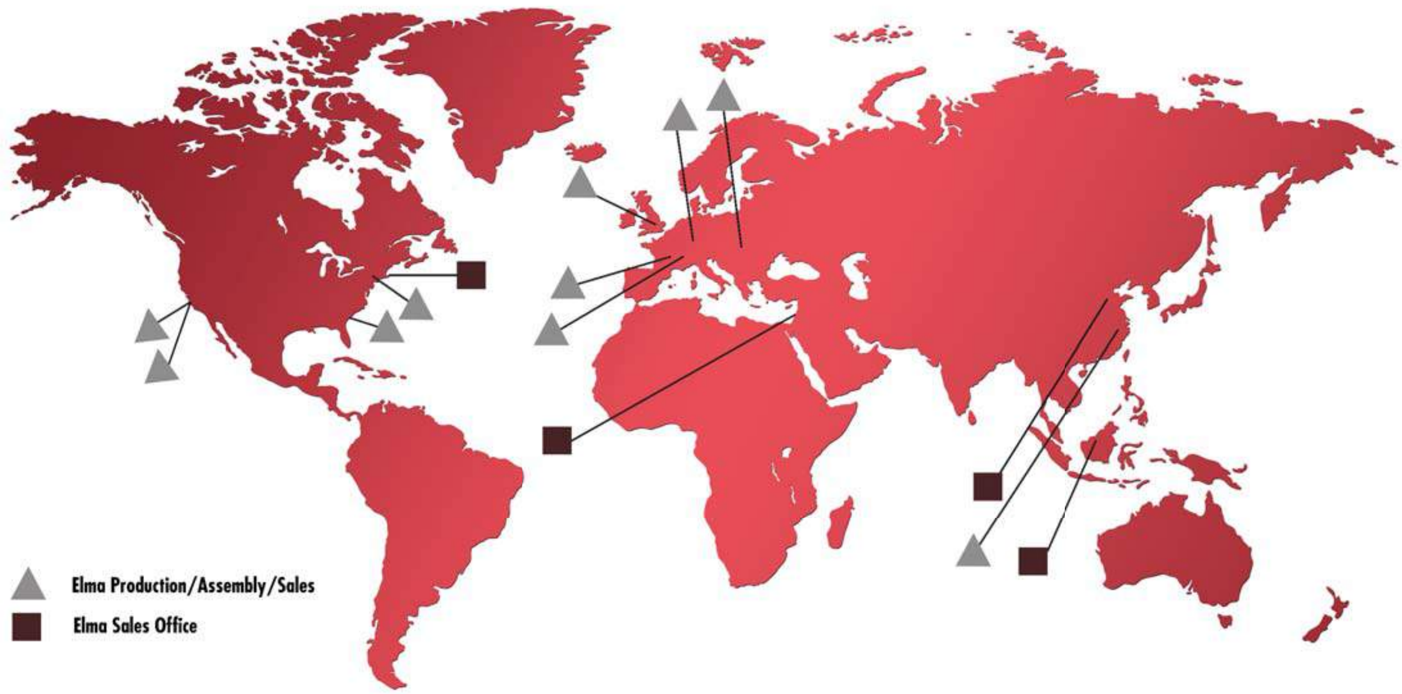
SerDes Test Devices

- Multilane differential serial fabric test unit
- Flexible design allows signal analysis for various architectures (VPX, ATCA, VXS, etc.)
- Lab-on-board eliminates need for acquiring a whole rack of equipment
- Directly evaluate true Gbps serial link BER performance
- Test and characterize entire mutli-lane serial fabric (PCIe, sRIO, GigE) with one device
- Achieve lowest cost of test and fastest time to market
- Can be used for testing both line cards and backplanes
- Test up to 16 channels at once, up to 6.4 Gbps
- Perform pre-emphasis tuning

The adoption of serial link technology in VPX and ATCA poses significant debug, characterization, and test challenges. The BTSD16 is an ultra low cost multi-lane Gbps serial test device that achieves unprecedented density and performance. With the BTSD16, you do not need to purchase equipment such as oscilloscopes, pattern generators, jitter analyzers, BERTs, clock generators, and analog function generators for higher speed testing. The device allows the user to characterize the PCIe, Gig E, sRIO, XAUI, or SATA ports quickly and efficiently. Speeds to KX and KX-4 are currently covered by the module, with a roadmap to KR levels. The BTSD16 uses cabling in the VPX, ATCA or other architectures. The unit is connected to a VPX backplane using a 24" VPX cable (full fat pipe connection wafer to SMA contacts and SMA adapter).

Order Information

Description	Channels	Order Number
BTSD16 Test Module with 2x VPX Cables (24", wafer to SMA & SMA adapter)	16	1940000511-0000
BTSD16 Test Module without cables	16	1940000508-0000
VPX Test Cables (1 set)	n/a	Contact Factory



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