VPX55-3HU 3U VPX Power Line Conditioner with Holdup

400 Watt, Ruggedized

VITA Front End Plug-in Module, Conduction-Cooled

Made in the USA
Certified Small Business

Description

NAI's VPX55-3HU are 400 Watt DC/DC power Line Conditioners which plug directly into a standard 3U VPX chassis with a VITA 62 0.8" or 1.0" power supply slot. This off-the-shelf solution is compatible with VPX specifications.

NAI's VPX55-3HU are +28V in DC power line conditioners with holdup capability which protect downstream DC-DC converters from Mil-Std 704 transients, low voltage conditions and power interruptions; providing up to 50 milliseconds of holdup time at 400 watts. The VPX55-3HU are designed to meet standard 3U VPX (VITA62) mechanical requirements and is a perfect companion unit for all NAI VPX +28Vdc DC/DC converters. This COTS conditioner is specifically designed with NAVMAT component derating for rugged defense and industrial applications. It is also designed to meet the many harsh environmental requirements of military applications.

Features

- Ideal for rugged 3U VPX power applications
- Standard VPX-compatible connector per VITA 62
- Compatible with System Management Bus per VITA 46.11
- Off-the-shelf solution for VITA 46.0 and VITA 65 systems
- Supports all VITA standard I/O, signals, and features
- Protects DC/DC Converters From Mil-Std 704B through F Transients
- Designed to work with the NAI VPX55-3 family of DC-DC Converters
- Wedgelock, Plug-in Design (conduction cooled)
- Reverse Polarity Protection
- Holdup
- Auxiliary Output
- BIT

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Electrical Specifications

DC Input Characteristics	
Input	+22Vdc to +30Vdc with Holdup capability. Operation down to +16Vdc with no Holdup capability.
EMI/RFI	Per MIL-STD-461F when used with additional system EMI filtering.
Input Transient Protection	Per MIL-STD-704B through F. - Ride through protection for: Normal Voltage Transients & Power Interrupts.
Reverse Polarity Protection	Shall not be damaged when subjected to reverse DC polarity on the input.
DC Output Characteristics	
Main DC Output Power	+40Vdc @ 400 watts maximum to downstream NAI DC/DC Converters.
Auxiliary Output	+3.3Vdc @ 1.0 Amp
Holdup Time	Up to 400 watts of primary power for up to 50millisecond.
Holdup Cap Replenishment Time	0.5 seconds.
Signals	
Vin_OK*	Monitors whether input voltage is within nominal range.
Holdup_OK*	Monitors whether the holdup capacitor is charged.
HU_FAIL*	Indicates internal failure in the unit. Signal complies with VITA 65 for active Low. FAIL* signal is Open Drain. It is expected that there will be a pull-up resistor on the backplane.
HU_ENABLE*	Turns off all the output voltages, including AUX, when signal is High. ENABLE* can be pulled Low by using a mechanical switch or other means which connects it to SIGNAL_RETURN. A Logic output can also be used to drive the ENABLE*. Opening the switch would turn off all the outputs; closing the switch or applying the Logic output would enable the outputs to come on depending on the state of INHIBIT*. An input of <0.8 VDC is regarded as a Low and an input of >2.0 VDC is regarded as a High. A no-connect is also regarded as a High. Along with INHIBIT*, this signal determines the output power status of the VPX55-3 (see Power Status Table below).
HU_INHIBIT*	Turns off the output voltage. The signal does not affect the 3.3 V_AUX. Pulling INHIBIT* Low turns off power to back end modules. An input of <0.8 VDC is regarded as a Low and an input of >2.0 VDC is regarded as a High. A no-connect is also regarded as a High. Along with ENABLE*, this signal determines the output power status of the VPX55-3 (see Power Status Table below).
Geographical Addressing	As defined in VITA 46.
Protocol	Per VITA 46.11 System Management Bus.

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Physical/Environmental Specifications	
Temperature Range	Operating: -40°C to +85°C at 100% load (temperature measured at card edge, conduction via card edge); Storage: -55°C to +100°C per VITA 47 CC4)
Reliability (MTBF)	100,000 hours, Ground Benign at 50°C Baseplate
Altitude	1,500 feet (below sea level) to +60,000 feet per VITA 47
Shock	30 G's each axis per MIL-STD-810G, Method 516.6, Procedure 1; Hammer shock per MIL-S 901, ½ sine wave per VITA 47 OS2
Acceleration	6 G's per MIL-STD-810G, Method 513.6, Procedure II
Vibration	Per MIL-STD-810G, Method 514.6, Procedure 1A
Humidity	95% at 71°C per MIL-STD-810G, Method 507.5 (non-condensing)
Salt & Fog	Per MIL-STD-810G, Method 509.5
Sand/Dust	Per MIL-STD-810G, Method 510.5
Fungus	Per MIL-STD-810G, Method 508.6
ESD	15 kV EN61000-4-2 per VITA 47
Enclosure	Aluminum housing to aluminum baseplate
Dimensions	Standard 3U, VITA 62, Single Card Slot 0.8" See Mechanical Layout
Finish	Chemical film IAW MIL-DTL-5541, Type II, Class 3
Interface	See Connector Specifications below
Weight	1.5 LBS TYPICAL (STD 0.8" Pitch)

All specifications are subject to change without notice.

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LED Status

LED STATE	MEANING
Off	Input out of nominal range
Green (Steady)	All outputs are good
Red (Steady)	FAIL; Follows the same logic as HU_FAIL* Signal
Blinking (**Green**)	Unit Disabled
Blinking (**Red**)	Over-Voltage or Over-Temperature (All outputs are off)

Power Status

Control Input States		Power Output States	
ENABLE*	**INHIBIT***	**+3.3V_AUX**	**Output**
High	High	Off	Off
High	Low	Off	Off
Low	High	On	On
Low	Low	On	Off

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I²C Communication

Description

I²C is a bi-directional, two wire serial bus which provides communication using a data line and clock line (SDA and SCL).

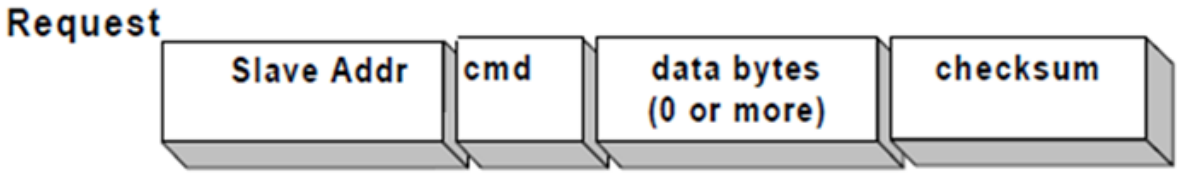
Using I²C Communication on NAI, VPX55-3 Power Supplies

1. Hardware Interface.
   Electrical interface is based on I2C parameters at 100 kHz. The backplane or I2C master controller should provide pull up resistors on SDA (Data) and SCL (Clock) lines to a 3.3V rail. On the NAI **VPX55-3,** the SDA line is located on Pin D5 (SM1) and the SCL line is located on pin C5 (SM0).

2. Address.
   The I2C Address is 7 bits. Default base address is 0x20. *GA0, and *GA1 provides 2 LSB's for the address.
   The *GA pins have pull-up resistors internal to the power supply to 3.3V. When left open, the address will be 0x20, with both grounded the address will be 0x23, see table below.

Pin		I2C Address
*GA1	*GA0	
Pin - B5	Pin - A5	
High	High	0x20
High	Gnd	0x21
Gnd	High	0x22
Gnd	Gnd	0x23

1. **Data Read - Get Sensor Reading results**



	Byte	Data Field	Data
Request Data	1	cmd	See table
	2 to n-1	Data If Required by cmd or Zero ChkSum* if no Data required.	
	n	Zero ChkSum* if Data was required by cmd	
Response Data	1	Completion Code – Echo cmd Number	
	2 to n-1	Per cmd Response	
	n	Zero ChkSum	

Note : Slave address should not be included in Zero Checksum calculation.

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2. Commands

Sensor #	Name	Description
21H	Composite Sensor	64 bytes of scanned sensor data. Data is continually scanned and available for report. Data consists of 2 bytes of data for each of the 11 sensors and FRU data.
55H	Status Write Command	Writes Status byte on Composite Sensor.
44H	Firmware release date	22 byte response. Month/Day/Year Hr/Min/Sec in ASCII form.
45H	Hardware Address	3 byte response. Reports address set by GA0*-GA1*

4.1 Composite Sensor Read Command – 21H

Response BYTE #	Data Type	Meaning
0	Completion Code – 21h	Echo of the command
1	Status Register 0, MS Bit	Refer to table below
2-3	Signed Integer, MSB First	Temperature as follows °C = (Reading * 100 / 16384)
4-5	U Integer, MSB First	Voltage on HU, 28V = 16384
6-7	U Integer, MSB First	Reserved
8-9	U Integer, MSB First	Reserved
10-11	U Integer, MSB First	Voltage on 3.3Aux, 3.3V = 16384
12-13	U Integer, MSB First	Reserved
14-15	U Integer, MSB First	Reserved
16-17	U Integer, MSB First	Current on HU, 20A = 16384
18-19	U Integer, MSB First	Reserved
20-21	U Integer, MSB First	Reserved
22-23	U Integer, MSB First	Reserved
24-25	U Integer, MSB First	Reserved
26-27	U Integer, MSB First	Reserved
28-29	U Integer, MSB First	Internal Reference, 2.5V = 16384
30-31	U Integer, MSB First	Input Voltage, 28V = 16384
32-51	Character String	Part Number
52-53	U Integer, MSB First	S/N Hi
54-55	U Integer, MSB First	S/N Low
56-57	U Integer, MSB First	Date Code (Year/Week)
58-59	U Integer, MSB First	Hardware Rev
60-61	U Integer, MSB First	Firmware Rev.
62	Reserved	Reserved
63	Zero Checksum	Value required to make the sum of bytes 0 to 62 add to a multiple of 256 (decimal).

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Status Reg 0		R/Set	R/Set	R/W	R/W	R/W	R	R
Bit	7	6	5	4	3	2	1	0
	x	FAIL	OTWarning	SWPriority	*SW Inh	*SW En	*HW Inh	*HW En

Bits 5 AND 6 (OTWarning - FAIL) are Read and write. They are clear at startup. User can set them with a Status Write command. Hardware will clear them if there is a fault.

Bit 4 (SWPriority) is Read and write. It is clear at Startup. When clear the unit will be controlled by the hardware enable and inhibit signals. When set, the unit will be controlled by the SW inhibit and enable signals.

Bits 3 and 2 (SWInh SWEn) are read and write. Their logic works the same as the logic for the hardware Enable and Inhibit.

*SWEnable	*SWInhibit	OUTPUTS
0	0	INHIBIT (3.3V Aux is On, all other outputs are off)
0	1	ON
1	0	OFF
1	1	OFF

Bits 1 and 0 (HWIn - HWEn) are read only. They show the state of *Enable and *Inhibit pins while SWPriority is low.

4.2 Status Write Command - 55H

BYTE #	Data Type	Meaning
0	U Character – 55H	Command
1	U Character	Data
2	Zero Checksum	Value required to make the sum of bytes 0 and 1 add to a multiple of 256 (decimal).

The command to write to Status byte is 55h, followed by 8-bit data then zero checksum.

Example: To send a command to clear the faults and turn on all the outputs, the following sequence must be sent.
55h 78h 33h;

55h is the command needed to write to status byte zero.
78h data for byte zero,

Bit 7 set: don't care bit.
Bit 6 set: FAIL signal is high, software will clear it if unit fails
Bit 5 set: OTWarning signal is high, software will clear it if unit is close to 75 degrees.
Bit 4 set: Software has priority to enable/disable unit.
Bit 3 set: SWInhibit is high
Bit 2 low: SWEnable is low.

33h Value to achieve a sum of zero.

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4.3 Firmware release date – 44H

Response BYTE #	Data Type	Meaning
0	Completion Code – 44H	Echo of the command
1-20	Character String	Date
21	Zero Checksum	Value required to make the sum of bytes 0 to 20 add to a multiple of 256 (decimal).

4.4 Hardware Address – 45H

Response BYTE #	Data Type	Meaning
0	Completion Code – 45H	Echo of the command
1	U Character	I2C Hardware Address
2	Zero Checksum	Value required to make the sum of bytes 0 and 1 add to a multiple of 256 (decimal).

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Pinout Designations (P1)

Pin #	Name	Pin #	Name
P1	-DC_IN	B5	GA1*
P2	+DC_IN	C5	SM0
LP1	CHASSIS	D5	SM1
A1	RESERVED	A6	RESERVED
B1	RESERVED	B6	RESERVED
C1	HOLDUP_OK*	C6	RESERVED
D1	RESERVED	D6	VIN_OK*
A2	RESERVED	A7	RESERVED
B2	HU_FAIL*	B7	RESERVED
C2	HU_INHIBIT*	C7	RESERVED
D2	HU_ENABLE*	D7	SIGNAL_RETURN
A3	RESERVED	A8	RESERVED
B3	RESERVED	B8	RESERVED
C3	RESERVED	C8	RESERVED
D3	RESERVED	D8	RESERVED
A4	HU_AUX*	P3	RESERVED
B4	HU_AUX*	P4	RESERVED
C4	HU_AUX*	P5	RESERVED
D4	HU_AUX*	LP2	P_Out_Rtn (PO2)
A5	GA0*	P6	P_Out (PO1)

*** When not using the +3.3Vdc_Aux Output, leave these pins disconnected on backplane**

Connector Specifications

Unit (P0)	Backplane (J0)
TE Connectivity P/N 2314578-2	TE Connectivity P/N 2309390-1

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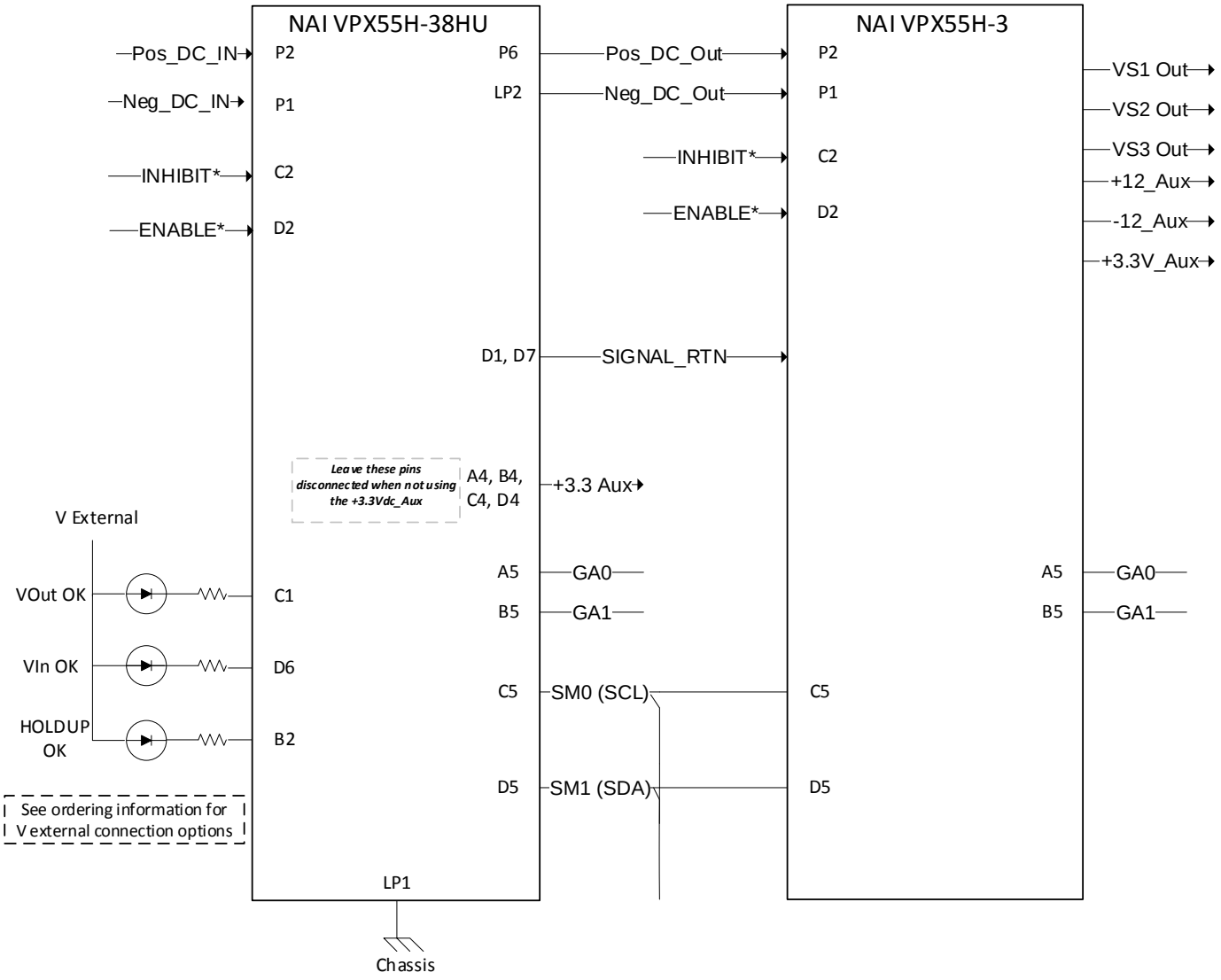
VPX55-38HU Connections



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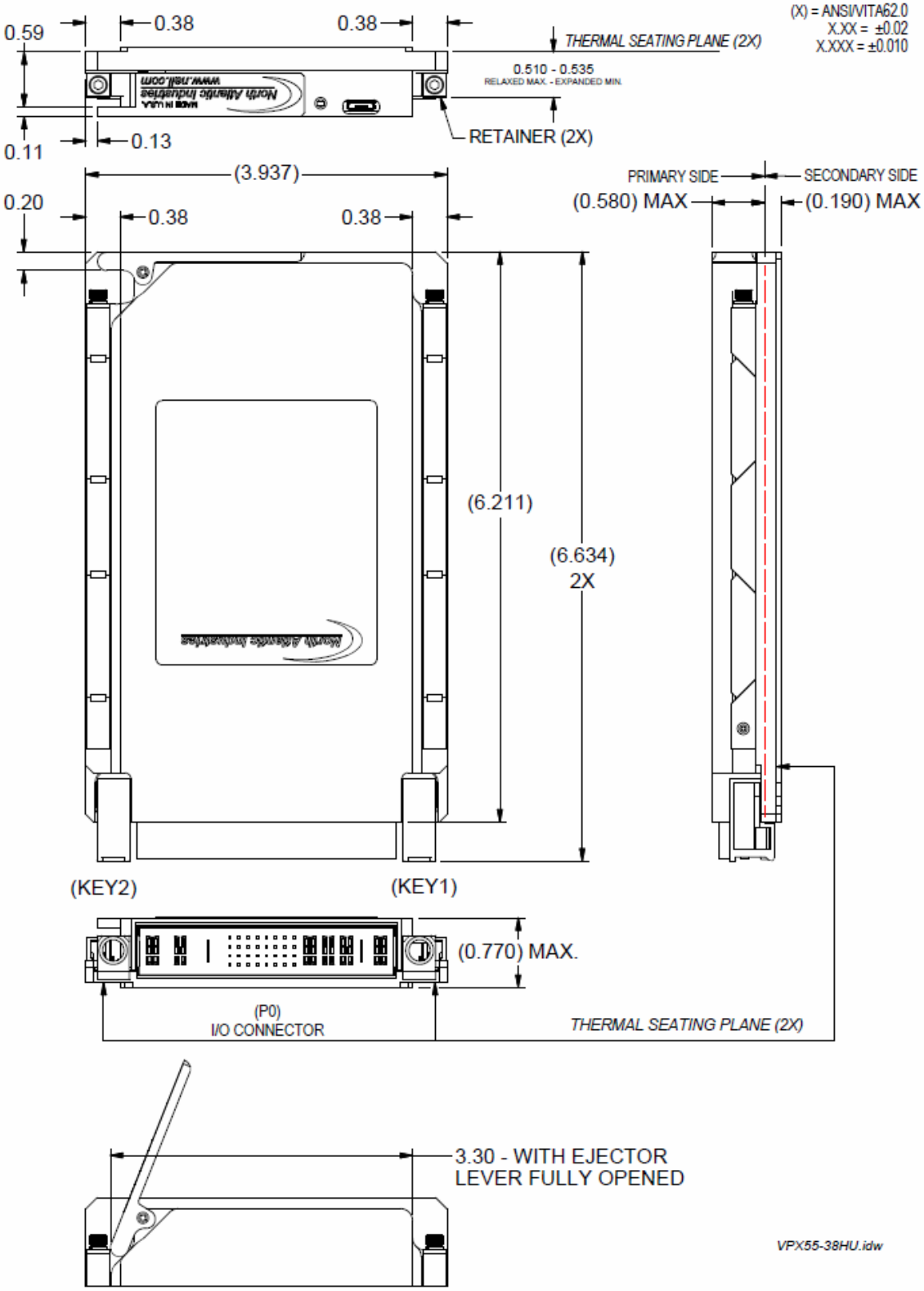
Mechanical Layout



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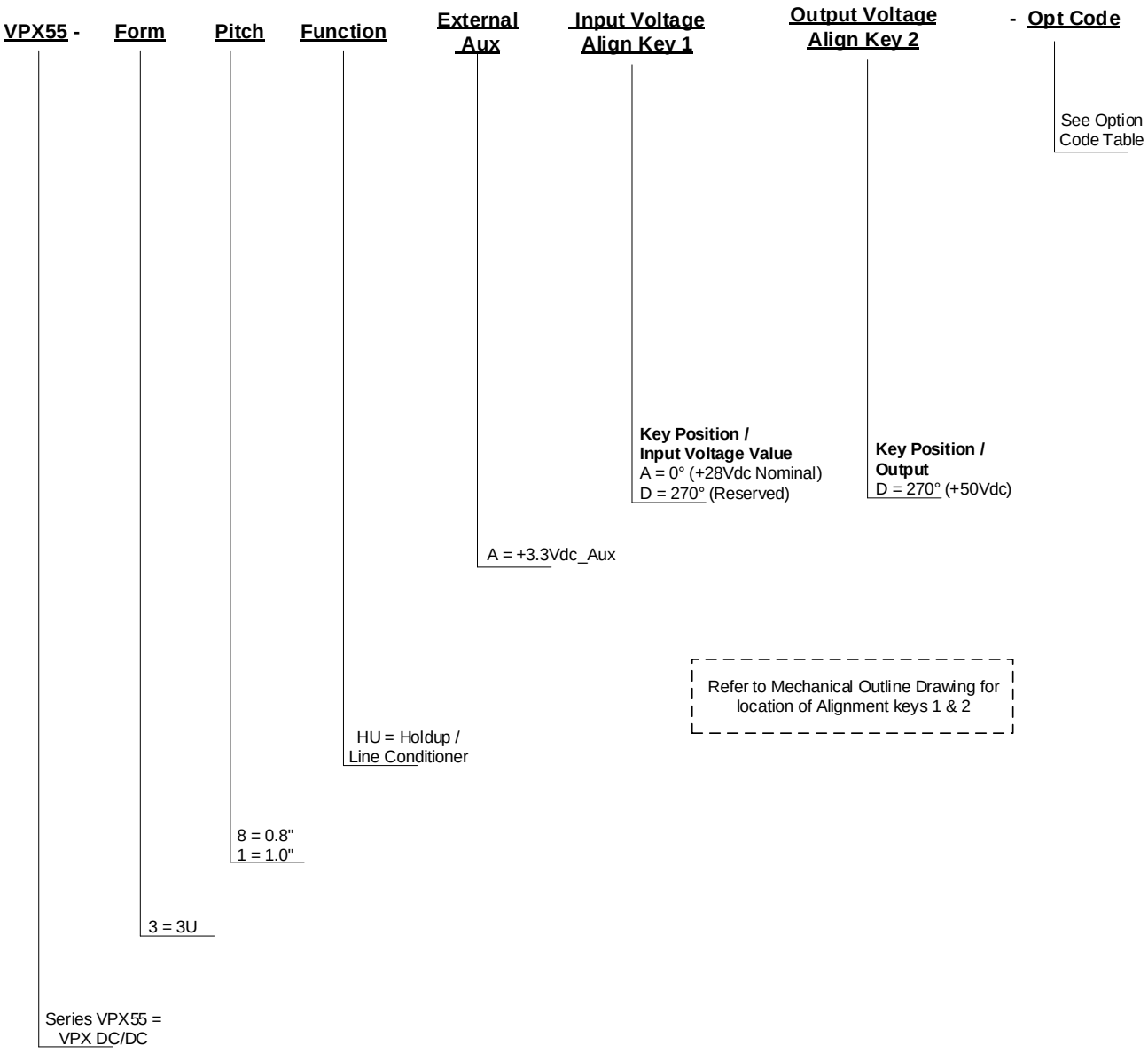
Ordering Information



Option Code Table

Code	Description
00	Standard unit, no additional options
01	Output of +36Vdc; Provides 350 Watts of Holdup Time for 50 milliseconds

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